# The SIDECAR ASIC — Focal Plane Electronics on a Single Chip

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## ABSTRACT

Traditionally, focal plane arrays require extensive external focal plane electronics (FPE) to provide clocks and biases as well as to digitize the analog output signals. The FPE has to be well-designed and is typically large, heavy and powerhungry. Most importantly, the FPE has to be placed some distance away from the FPA, which complicates maintaining low noise performance throughout the complete system. To offer an alternative to the discrete electronics, Rockwell Scientific has developed a new approach known as the SIDECAR application-specific integrated circuit (ASIC). This single chip provides all the functionality necessary to operate an infrared array with the convenience of a pure digital interface to the outside world. This paper will present performance data on the latest generation of the SIDECAR ASIC operating the JWST H2RG detector arrays at cryogenic temperature. The test results demonstrate that an ASIC based FPA system will meet or exceed all performance requirements for the JWST mission. The SIDECAR ASIC has been selected by NASA to become the FPA drive electronics for all shortwave infrared instruments on JWST.

**Keywords:** ASIC, SIDECAR, Focal Plane Electronics, HAWAII-2RG, Focal Plane Array, A/D Conversion

## 1. INTRODUCTION

The rapid progress of CMOS technology over the past decades has enabled significant improvements in the CMOS-based detector field. Monolithic CMOS image sensors for visible light can be found in many modern consumer applications, and hybrid CMOS sensors for a wide variety of wavelength from x-ray to long-wave infrared achieve multi-mega-pixel resolution in the high performance scientific community. Not only have the sensor properties improved, deep submicron CMOS has also pushed the miniaturization of integrated support electronics, which is an essential part of any camera system.

Conventional high performance image sensors, also called focal plane arrays (FPAs), require significant external control and support electronics. To reduce the amount of external overhead, more and more modern image sensors include the drive electronics on the sensor chip itself. This approach has been strongly endorsed by the consumer market where cost and miniaturization are strong drivers. Nowadays, complete camera solutions on a single chip can be found quite frequently (Bock et al. [1]). In the scientific arena, however, performance and flexibility remain the highest priority. Most astronomy detector systems are still based on analog FPAs operated by a dedicated controller box.

To offer an alternative to the discrete electronics, RSC has developed a new approach known as the SIDECAR™ application-specific integrated circuit (ASIC) as presented in Loose et al. [2]. The SIDECAR design includes all capabilities needed to operate the FPA, including bias and clock generation as well as A/D conversion. The interface to the outside world is fully digital, thereby simplifying the design of the instrument while guaranteeing constant low noise performance. Overall, the ASIC approach leads to a hundredfold reduction in space, weight and power consumption.

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## 2. SIDECAR ARCHITECTURE

The SIDECAR ASIC is a fully programmable control and digitization system for analog image sensors. It is designed to operate at room temperature as well as at cryogenic temperatures down to 30 K. Figure 1 shows a block diagram of a typical ASIC-driven detector system. The top block represents the FPA, which is connected to the ASIC (center block) via many analog and digital wires. At the bottom of the ASIC block, only digital wires go to the external data acquisition system. Due to the immunity of the digital signal transmission which can be LVDS or LVCMOS, the acquisition system can be located several meters away from the ASIC. The basic SIDECAR architecture, as shown in the diagram, can be divided into the following major blocks: analog bias generator, A/D converter, digital control and timing generation, data memory and processing, and digital data interface.

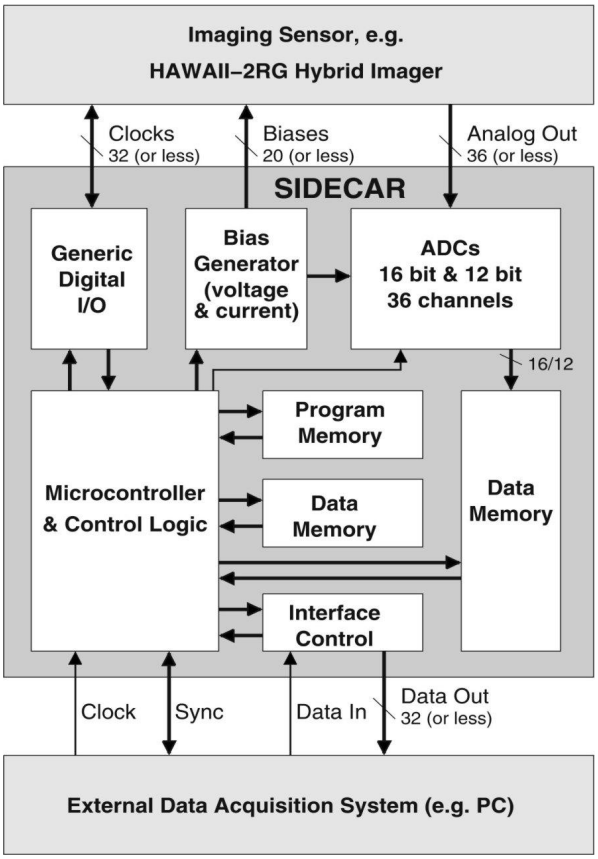


Figure 1: Block diagram of the SIDECAR ASIC.

The analog bias generator consists of 20 independent channels, each of which is composed of a 10-bit digital-to-analog converter and an output buffer with adjustable driver strength. Each channel can be used as a programmable current and voltage source. For reading out the analog detector signals, the ASIC provides 36 analog input channels. Each channel can be digitized by on-chip ADCs offering 16-bit resolution at sample rates up to 500 kHz and 12-bit resolution at sample rates up to 10 MHz. A fully programmable and application optimized micro-controller is responsible for the overall ASIC control and for generating the specific timing patterns of the image sensor clocks. A total of 32 digital I/O channels can be individually adjusted for driver strength and signal direction. Additional on-chip memory permits simple data processing functions like pixel averaging or data sorting. Finally, serial and parallel data interfaces are implemented to read the digitized pixel values and to program the ASIC.

The primary driver for this controller-on-a-chip approach was the development of the James Webb Space Telescope (JWST), successor to the Hubble Space Telescope. The necessity of 16-bit accuracy at a temperature of 37K without active cooling put stringent requirements on the performance and power consumption of the ASIC. The JWST goal is 16-bit conversion on 4 parallel channels at a power consumption of less than 10 mW, including bias generation, clock generation and data transmission. As the next section describes, this goal has been achieved. The SIDECAR ASIC is fully suitable for JWST and other space-based applications, as well as for ground-based applications.

Figure 2 shows a micrograph of the SIDECAR chip as well as a packaged ASIC in a 337-pin µPGA package. The dimensions of the ASIC die amount to 22mm x 14.5mm. About 2/3 of the area are taken by the 36 mixed-signal data channels consisting of preamplifier, ADC, array processor and data memory. A summary of the important ASIC properties is given in table 1.

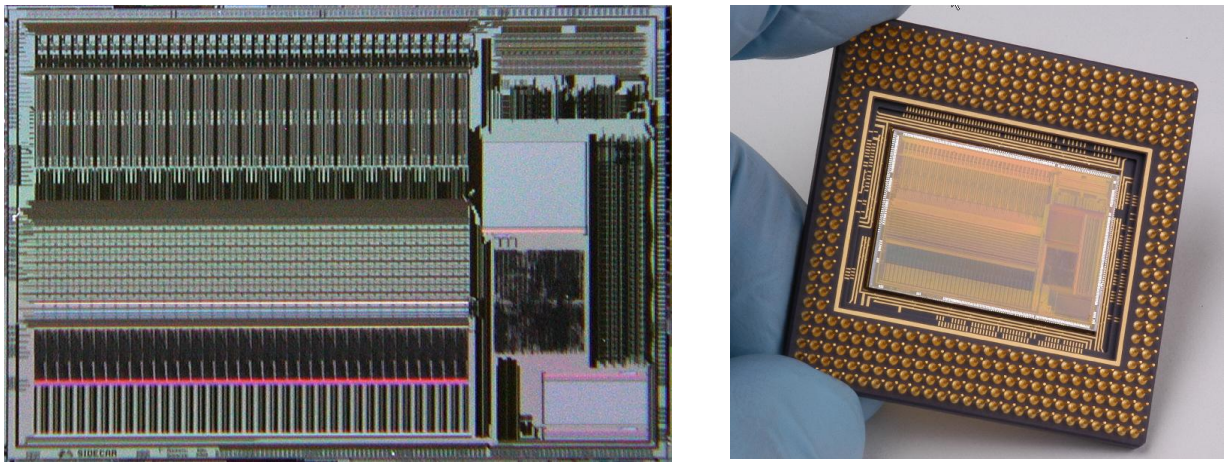

Figure 2: Micrograph (left) and packaged SIDECAR ASIC (right)

Table 1: Summary of the SIDECAR ASIC properties

| | |
|---|---|
| Die Dimension | 22 x 14.5 mm² |
| Technology | 0.25 µm CMOS |
| Analog Input | 36 independent channels, fully differential |
| Preamplifiers | Programmable gain (-3 to 27 dB) and bandwidth |
| 16 bit ADCs | Up to 500 kHz sample rate (1 mW / channel at 100 kHz) |
| 12 bit ADCs | Up to 10 MHz sample rate (10 mW / channel at 5 MHz) |
| Bias Outputs | 20 output channels, selectable voltage or current DACs |
| Digital I/O | 32 channels, fully programmable |
| Micro-controller | 16 bit RISC, low power, excellent arithmetic capabilities |
| Program Memory | 16 kwords (16 bit / word) |
| Data Memory (µC) | 8 kwords (16 bit / word) |
| Data Memory (ADC) | 36 kwords (24 bit / word) |
| Array-processor | Adding & multiplying and DMA control per ADC channel |
| Digital Interface | LVDS or CMOS, custom serial protocol, up to 32 parallel lines |
| Operating Temperature range | 30 K – 300 K |
| Radiation | Complete design is single event upset protected |

## 3. MEASUREMENT RESULTS

The performance and functionality of the SIDECAR ASIC have been examined at room temperature (presented in Wong et al. [3]) and at cryogenic temperatures down to 37 K. Room temperature performance is important for applications that operate the detectors at or near room temperature (visible light and/or high background) as well as for convenient testing and verification of the ASIC itself. On the other hand, cryogenic performance is essential for low background detector systems that benefit from analog to digital conversion close to the FPA.

The test results will be presented in the following three sections. The first section describes the performance of the individual ASIC components such as ADCs and preamplifiers. In the subsequent section, cryogenic results from radiation tests with protons will be discussed. The third section covers the most comprehensive tests to date: the measurement results from a complete system test comprising the SIDECAR ASIC and the HAWAII-2RG at cryogenic temperatures. Both types of results have been obtained using a PC-based environment with a custom-built test board. Room temperature tests have been carried out at Rockwell Scientific; cryogenic tests have been performed at the Institute for Astronomy in Hilo, Hawaii.

### 3.1. SIDECAR ASIC Functionality and Performance Results

The purpose of the first set of tests included the verification of the correct functionality and the measurement of the analog performance of all integrated building blocks. As part of these initial tests, the test environment had to be completed and various ASIC micro-code programs had to be written. Aside from a leakage problem in one of the integrated memory modules, all digital and analog components were fully functional. Subsequently, fabrication of a second ASIC revision has completely solved the problem in the memory module. The following paragraph lists all building blocks that have been measured and verified:

- Serial/parallel data interface to and from SIDECAR
- Micro-controller plus program and data memories
- Timer/Counter modules
- Digital I/O block for clock generation
- Array processor for parallel data processing
- Analog bias generator for internal/external voltage and current biases
- Integrated 2.5V voltage regulator for digital supply voltage
- 12-bit ADC, DNL < ± 0.3 LSB, INL < ± 0.8 LSB, noise < 0.4 LSB
- 16-bit ADC, DNL < ± 0.4 LSB, INL < ± 2.3 LSB, noise < 3 LSB
- Preamplifiers, noise at T=300K: 20μV, noise at T=40K: 12μV

The analog performance of the two types of on-chip ADCs has been examined with respect to linearity and noise. In the case of the 12-bit ADC, the differential and integral nonlinearities (DNL and INL) at a sample rate of 7.5 MHz are shown in Figure 3. At room temperature and at T=40K, the 12-bit ADCs exhibit excellent DNL and INL as well as low temporal noise of less than 0.4 LSB. No significant difference in performance has been observed for sampling rates of 1-10 MHz.

Likewise, the 16-bit ADC shows good performance with respect to DNL and INL (Figure 4). In terms of noise, a compromise between the noise level and the power consumption suitable for JWST had to be found. At a power level of 1.3 mW and a sampling rate of 100 kHz, the ADC noise is 5 LSB at room temperature and 2.5 LSB at T=40K. This performance fulfills the JWST requirements with margin. The noise can be further improved by increasing the ADC bias current at the cost of higher power consumption. However, no measurements at higher bias conditions have been undertaken.

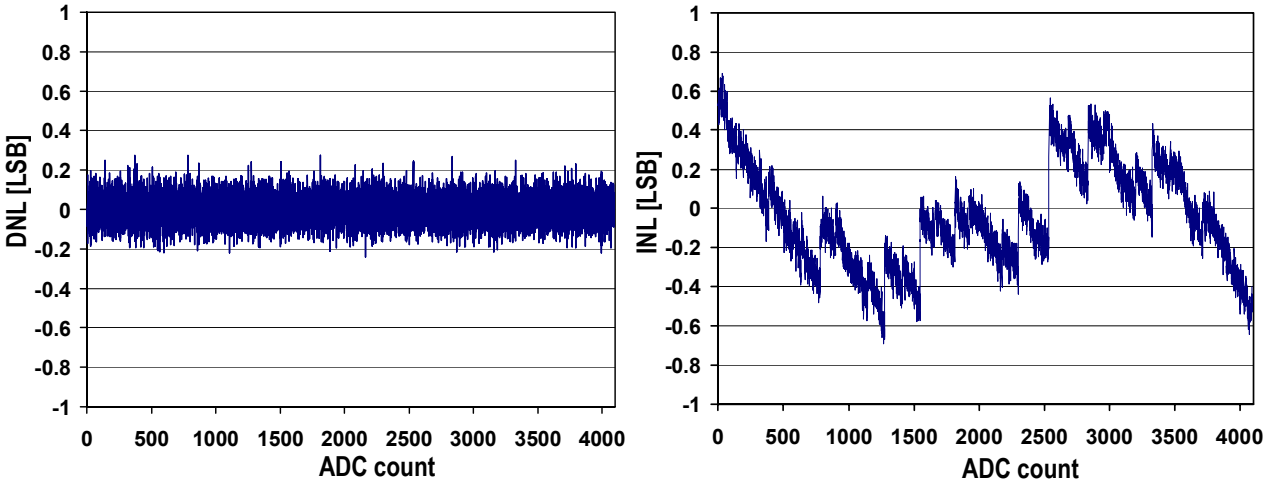


Figure 3. DNL (left) and INL (right) of the integrated 12-bit ADC (7.5 MHz).

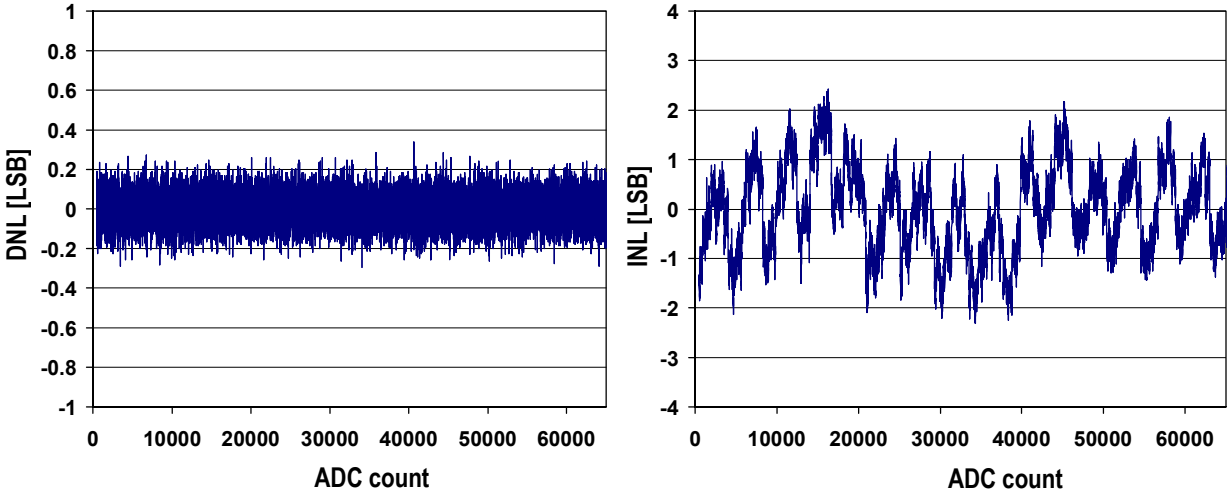


Figure 4. DNL (left) and INL (right) of the integrated 16-bit ADC (100 kHz).

The preamplifier provides control over the analog signal gain and the analog signal bandwidth by means of programmable capacitors and resistors. Its performance has been evaluated under JWST conditions for 100 kHz pixel rate, using a bandwidth of 300 kHz and a gain of 27 dB. The measured noise is to 20μV (input-referred) at room temperature and less than 12μV at 40K. Combining the noise of the preamplifier and the noise of the 16-bit ADC results in a total analog noise of 18μV for cryogenic operation. As mentioned above for the ADC, increasing the bias current (power consumption) can further reduce the amplifier noise.

### 3.2. Radiation Test Results

The ASIC has been designed specifically for space-based applications and consequently must comply with radiation requirements for both total dose and single event effect. A number of design features have been implemented to ensure proper operation under typical space environments. Since the ASIC is solely in charge of the detector operation, a single event upset (SEU) in the logic could lead to a serious malfunction of the whole detector system. For that reason,

preventing SEUs from occurring at all became a priority. All critical circuit including the logic (e.g. microcontroller), the memories and the configuration registers have been SEU hardened by design.

The SIDECAR ASIC has undergone radiation testing with 63 MeV protons while being operated at the typical JWST temperature of 37K. Over the course of the tests, a total dose of 80 krads has been accumulated without any noticeable degradation in performance. During the duration of the test, the integrity of the ASIC and its internal microcode were continually monitored to detect any possible single event effects. The results demonstrate that the design is extremely robust: After a total flux of $1.6*10^{12}$ protons/s/cm$^2$, only a single upset was found that caused incorrect operation and required a system reset. Scaling this probability to JWST-like fluxes, the expected rate for SEUs is less than 1 occurrence per 10,000 years.

In addition to the digital SEU rate, artifacts in the analog behavior caused by the proton radiation have been examined. Figure 5 shows the histograms of about 20000 ADC samples taken at 100kHz sample rate. During the 2-second experiment, the analog input voltage to the preamplifier was kept constant. As expected, the histogram exhibits a Gaussian noise distribution, which can be seen in the left histogram. This behavior does not change, even at a proton flux of 6000 p/s/cm$^2$. However, increasing the flux to $3*10^8$ p/s/cm$^2$ causes the single Gaussian peak to separate into multiple peaks (right histogram). The reason is that the charge generated by the incident proton can get injected into the feedback capacitor of the preamplifier and thus shift the baseline by a small amount. This baseline shift occurred about 4 times and resulted in 5 different peaks.

In principle, this effect can be eliminated by resetting the preamplifier every ADC cycle. On the other hand, the probability for this baseline shift to occur is extremely small (about one occurrence per year under JWST-like fluxes) and should not be of any concern even with a much lower reset rate.

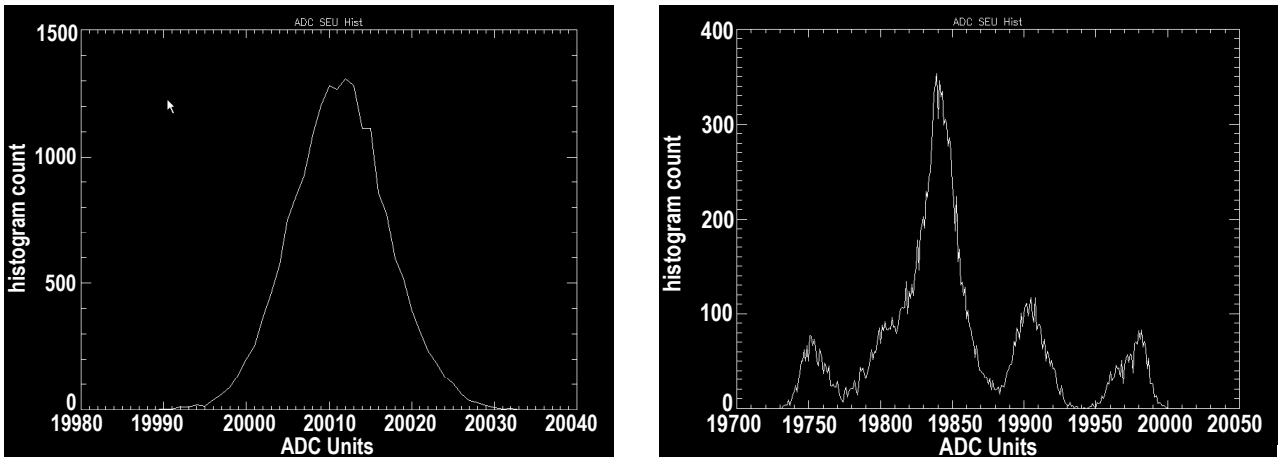


Figure 5: Histograms of about 20000 ADC samples of a constant analog input voltage amplified by the built-in preamplifier. The left picture shows data taken at low proton flux, the right picture at high proton flux.

### 3.3. Performance of SIDECAR + HAWAII-2RG

To demonstrate the ASIC performance under real operating conditions, a complete detector system consisting of the SIDECAR ASIC and the HAWAII-2RG multiplexer has been assembled. Figure 6 shows a block diagram of the system configuration. The HAWAII-2RG, hybridized to a short-wave infrared detector with 2.5µm cutoff frequency, has been mounted next to the ASIC inside the dewar and was operated in unbuffered mode. The SIDECAR ASIC was programmed to generate the required bias voltages and clock signals. At the same time, the SIDECAR digitized the four analog FPA outputs at 100 kHz pixel rate and sent the digital data to the host PC.

During the noise test the power supply going to the ASIC showed significant voltage ripple. For that reason, initial noise results were on the order of 100 e- for a single CDS. However, the voltage ripple could be mitigated without changing anything in the test setup. A simple reconfiguration of the ASIC allowed operation of the HAWAII-2RG in differential mode (signal output and reference output) as opposed to single-ended mode, which reduced the power supply induced noise to negligible levels. All data presented below was obtained using the differential approach.

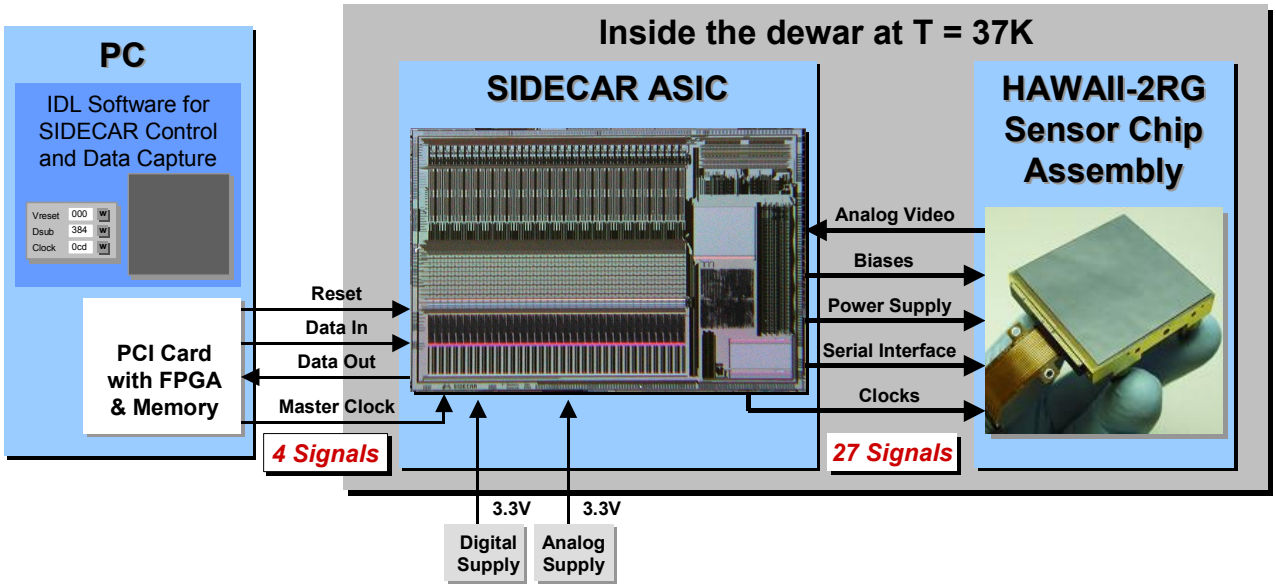


Figure 6. Block diagram of the cryogenic test setup including the SIDECAR ASIC and the HAWAII-2RG detector.

Figure 7 shows a full field CDS frame with a total noise of 16 e-. This is comparable to or better than results obtained with a conventional discrete controller system. To demonstrate suitability for the JWST instruments, the total noise had to be measured for a Fowler-8 sampling scheme (NIRCam) and for the sampling-up-the-ramp scheme with 22 groups of 4 averaged frames (NIRSpec). Fowler-8 refers to an 8-fold oversampling of the reset and signal frame which reduces the read noise by the square root of 8. Sampling-up-the-ramp corresponds to a scheme that continually reads one frame after another over the course of the whole integration time and calculates the signal per pixel by fitting a line to the collected data. The gray-scale images and the corresponding histograms are shown in Figure 8 and Figure 9. All JWST noise requirements have been met with margin.

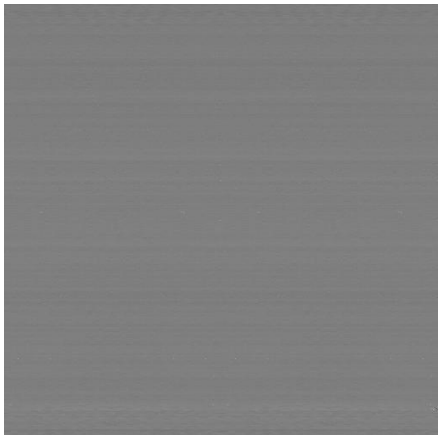

Figure 7. CDS frame acquired by the SIDECAR ASIC shows 16 e- noise.

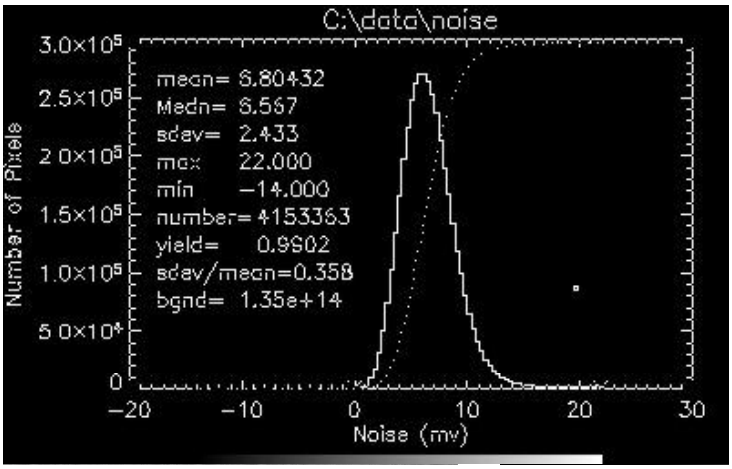


Figure 8. Fowler 8-8 over a 1000s integration yields a total noise of 6.5 e-.

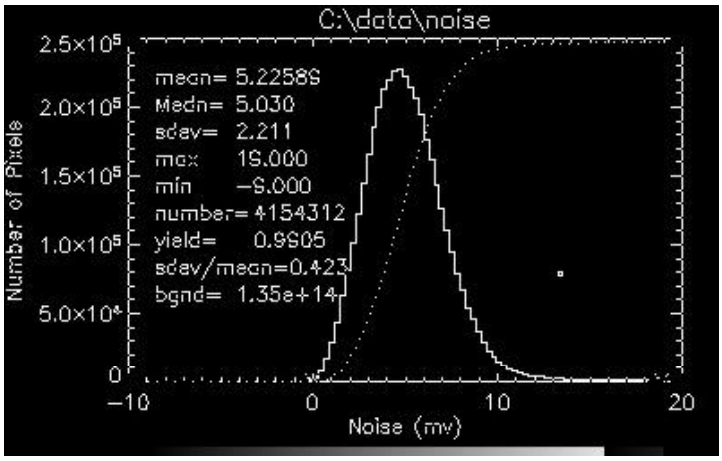


Figure 9. Sampling-up-the-ramp over 1000s integration yields a total noise of 5 e-.

In addition to the given examples of Fowler-8 and sampling-up-the ramp, the general noise value as a function of the number of Fowler samples has been examined. Theoretically, the noise should decrease as the square root of the number of samples. However, that is true only if the noise sources are completely white and statistically independent. In reality, the read noise is a combination of many noise sources with different properties, and the reduction with oversampling is typically less than the theoretical value. Figure 10 shows the measured noise performance as a function of samples, starting with about 16 e- for a single CDS (red curve). It can be seen that 4 e- noise is possible when averaging 64 Fowler pairs. The blue curve in the same diagram represents the theoretical noise reduction, assuming the same initial CDS noise of 16 e-. For Fowler-64, it predicts a read noise reduction down to 2 e-.

Besides noise performance, power consumption is important in many cryogenic detector systems. For JWST, a total budget of less than 10 mW has been allocated for each 2K x 2K detector to allow for passive radiative cooling. Table 2 summarizes the measured power consumption for all contributors inside the ASIC and the HAWAII-2RG. A total power of 9.4 mW has been demonstrated when operating in 4 channel mode with a pixel rate of 100 kHz per channel while applying 16-bit A/D conversion.

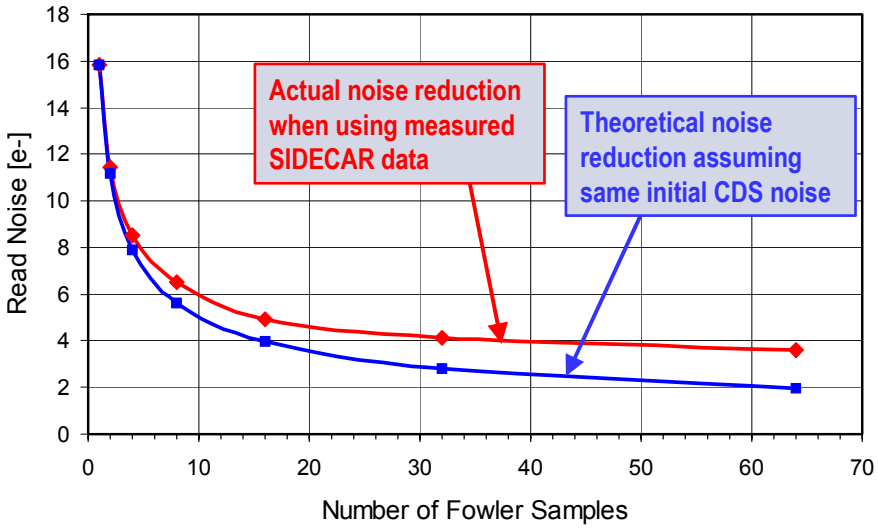


Figure 10. Comparison between theoretical noise reduction and measured noise reduction as a function of number of Fowler samples.

Table 2. Power consumption for operation with 4 channels including H2RG detector.

| Component | Power Consumption |
|---|---|
| HAWAII-2RG | 0.4 mW |
| 16-bit ADCs (4 channels) | 5.2 mW (1.3 mW / channel) |
| Preamplifiers (4 channels) | 1.0 mW (0.25 mW / channel) |
| Bias generator | 1.2 mW |
| Micro-controller & Clocking | 1.5 mW |
| LVDS Driver | 0.1 mW |
| **Total Power** | **9.4 mW** |

## 4. CONCLUSION

As presented in this paper, the SIDECAR ASIC is a fully integrated solution for operating FPAs: focal plane electronics on a single chip. Because of its high level of programmability, the SIDECAR can be used with many different detectors and supports all features of the Rockwell Scientific astronomy FPAs. Excellent performance has been measured at room temperature and at 37K. Noise results are comparable to or better than what is achieved with conventional controllers and in all cases meet or exceed the JWST requirements.

Based on the test results, NASA has selected the SIDECAR ASIC for use in all three JWST near-infrared instruments. Recently, a second ASIC revision was produced to correct a remaining leakage problem with the on-chip dual-port memory. The first SIDECAR ASICs of the new revision have been tested at Rockwell Scientific. The absence of excess leakage indicates that the memory leakage issue has been solved. The SIDECAR is in the process of becoming fully space-qualified, which includes the development of suitable packaging, application specific micro-code and further performance tests. The SIDECAR ASIC has proven to be an attractive alternative to conventional controllers for ground-based and space-based applications.

## 5. References


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