SIDECAR ASIC Characterization

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Background

- Developed by Teledyne Scientific & Imaging, LLC
- Generates the necessary clock signals and bias voltages while simultaneously digitizing imaging sensor outputs
- Reduced size and mass of control electronics is crucial in space missions which have mass limits
- Planned for use on the Hubble Space Telescope and the James Webb Telescope
- Configuration for optimal performance demands a high level understanding of its operation and firmware design

Goals

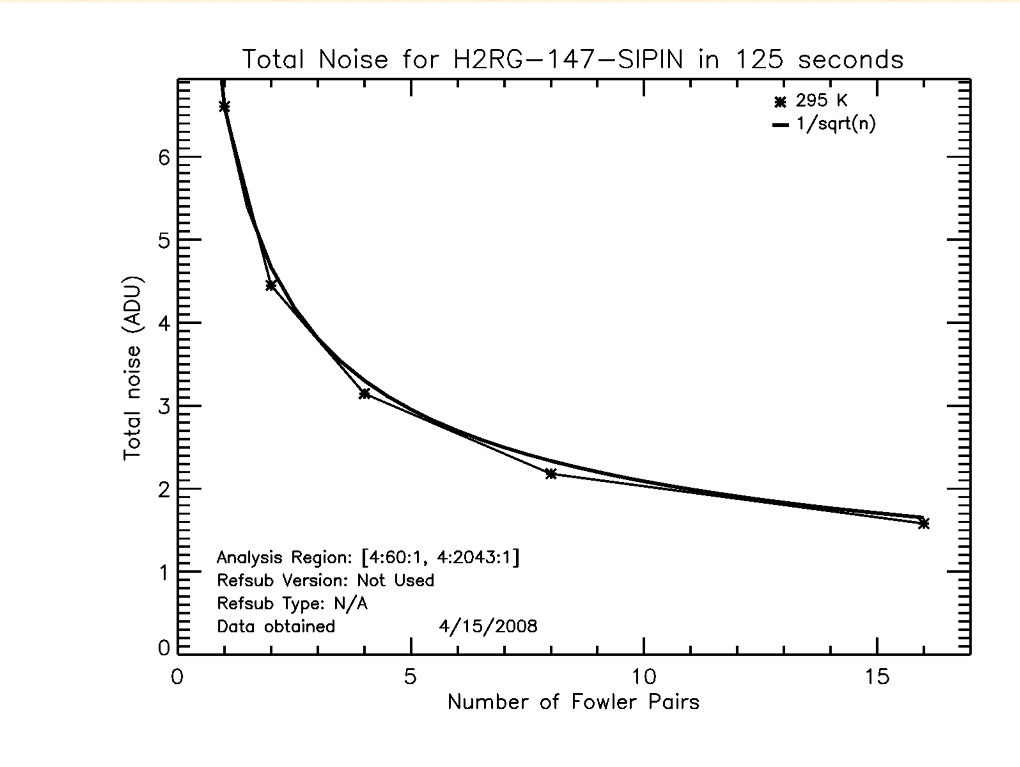
- Full evaluation and characterization of SIDECAR chip
- Efficient, optimized firmware
- Specifications for optimal experimental setups

Plan

- Obtain a baseline setup for minimal noise and processing
- Measure standard digitization characteristics
- Measure performance with respect to altered operational modes
- Organize performance data and specifications into a datasheet

Results

- Reduced read noise and improved image quality
- Simplified firmware and optimized readout performance



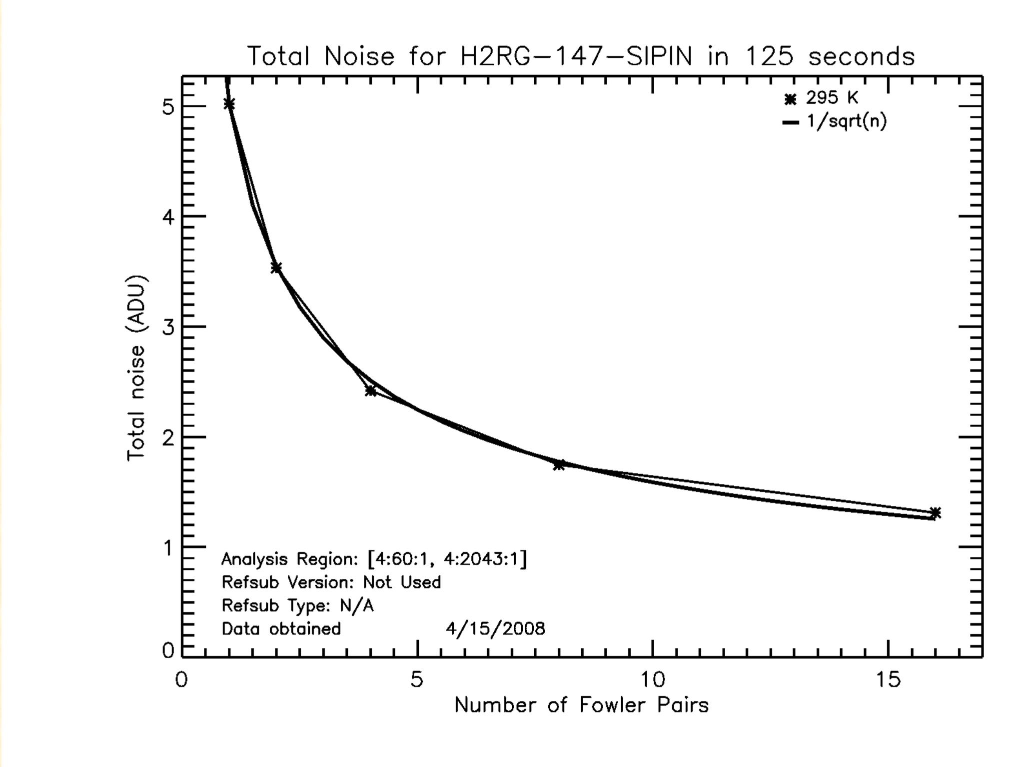


Figure 1: SIDECAR read noise results from two distinct setups in an experiment to remove a noise pattern. In this experiment, one input channel on the SIDECAR was fed a 1V DC signal from a power supply. **Right**: The SIDECAR was powered by a DC adapter via the USB cable. **Left**: The SIDECAR was powered by the laptop battery via the USB cable. The noise difference in the two setups can be attributed to the power source for the ASIC.

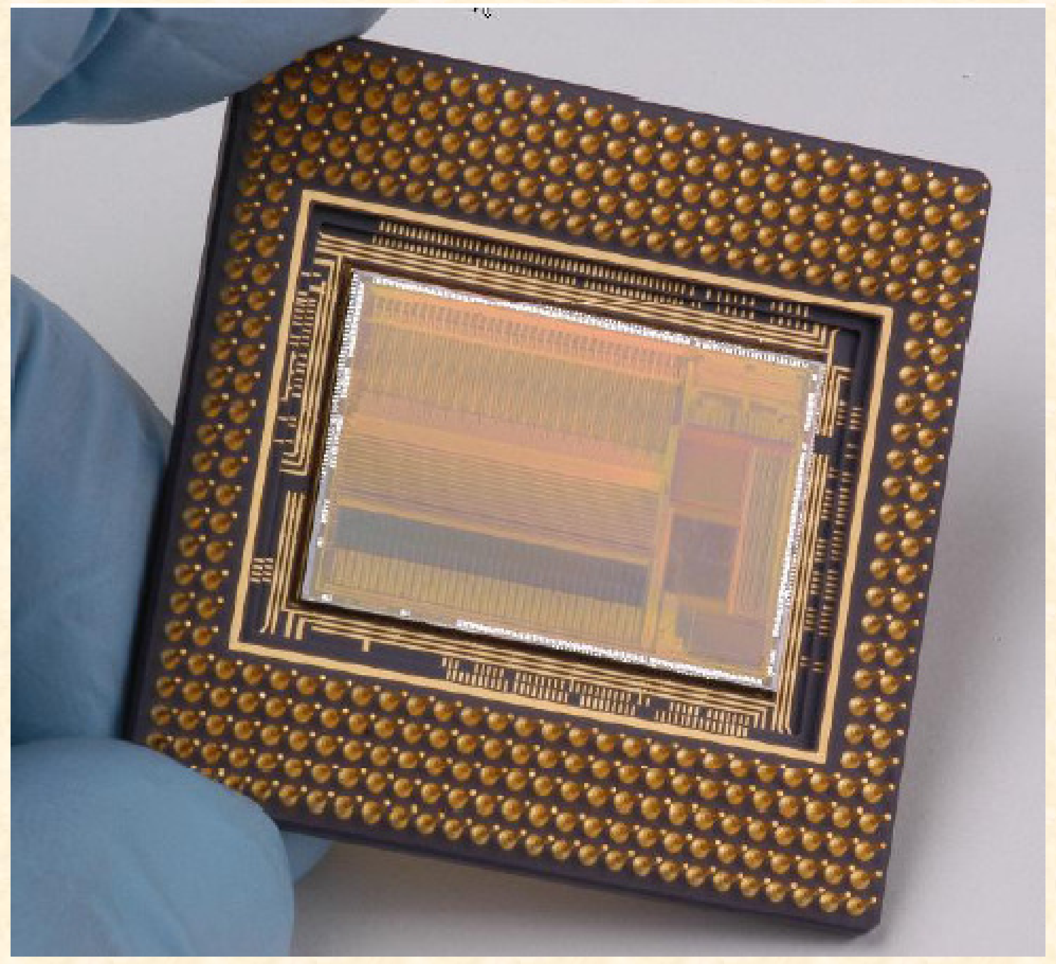


Figure 2: Image of the SIDECAR. All signal conditioning, clock/bias generation and digitization hardware is self-contained in this small chip.

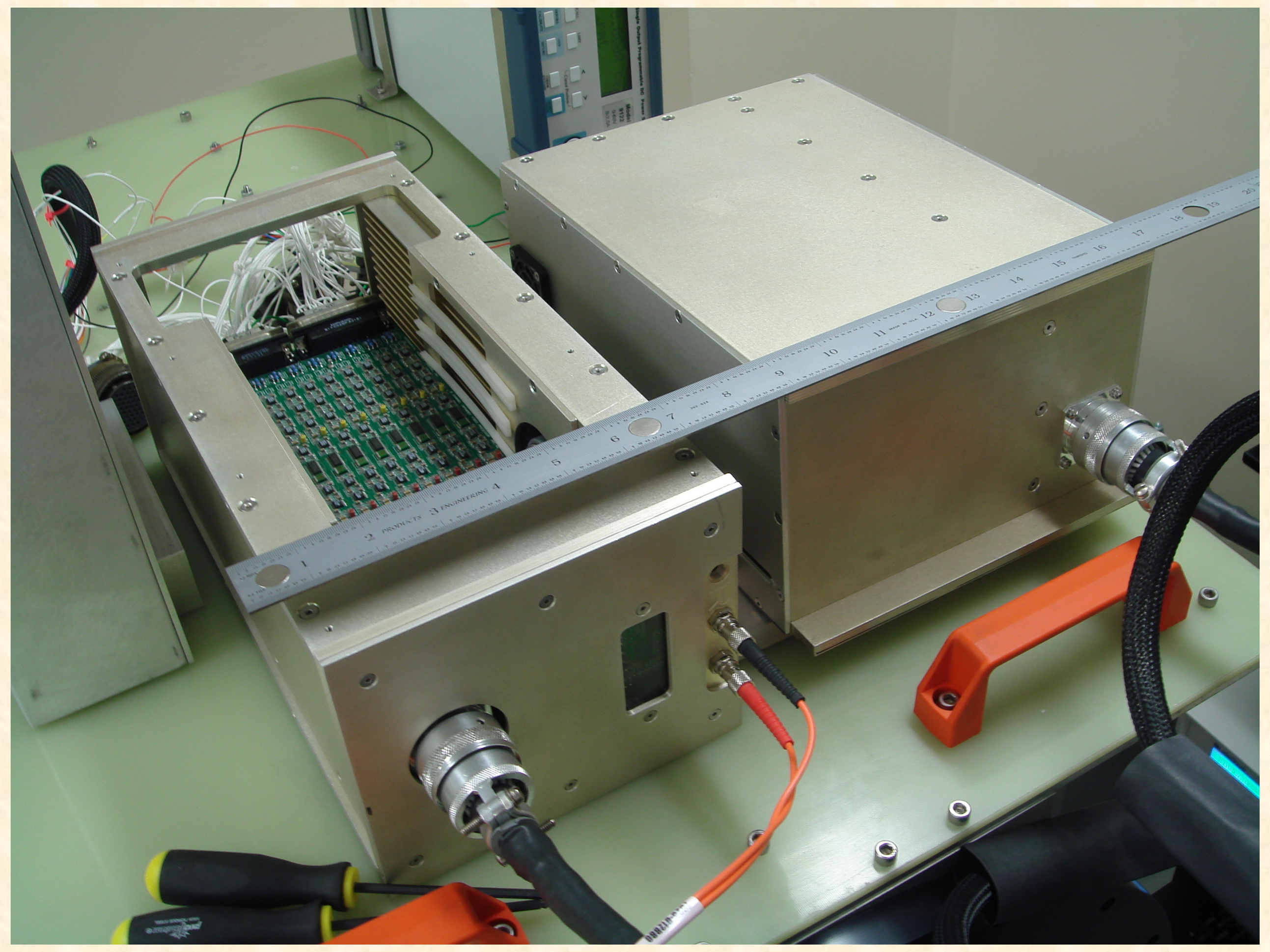


Figure 3: Detector control electronics built by Astronomical Research Cameras, Inc. The SIDECAR has the same capability as this set of electronics.

Table 1: Summary of the SIDECAR ASIC properties

Die Dimension	22 x 14.5 mm²
Technology	0.25 µm CMOS
Analog Input	36 independent channels, fully differential
Preamplifiers	Programmable gain (-3 to 27 dB) and bandwidth
16 bit ADCs	Up to 500 kHz sample rate (1 mW / channel at 100 kHz)
12 bit ADCs	Up to 10 MHz sample rate (10 mW / channel at 5 MHz)
Bias Outputs	20 output channels, selectable voltage or current DACs
Digital I/O	32 channels, fully programmable
Micro-controller	16 bit RISC, low power, excellent arithmetic capabilities
Program Memory	16 kwords (16 bit / word)
Data Memory (µC)	8 kwords (16 bit / word)
Data Memory (ADC)	36 kwords (24 bit / word)
Array-processor	Adding & multiplying and DMA control per ADC channel
Digital Interface	LVDS or CMOS, custom serial protocol, up to 32 parallel lines
Operating Temperature range	30 K – 300 K
Radiation	Complete design is single event upset protected

Figure 4: SIDECAR performance specification table

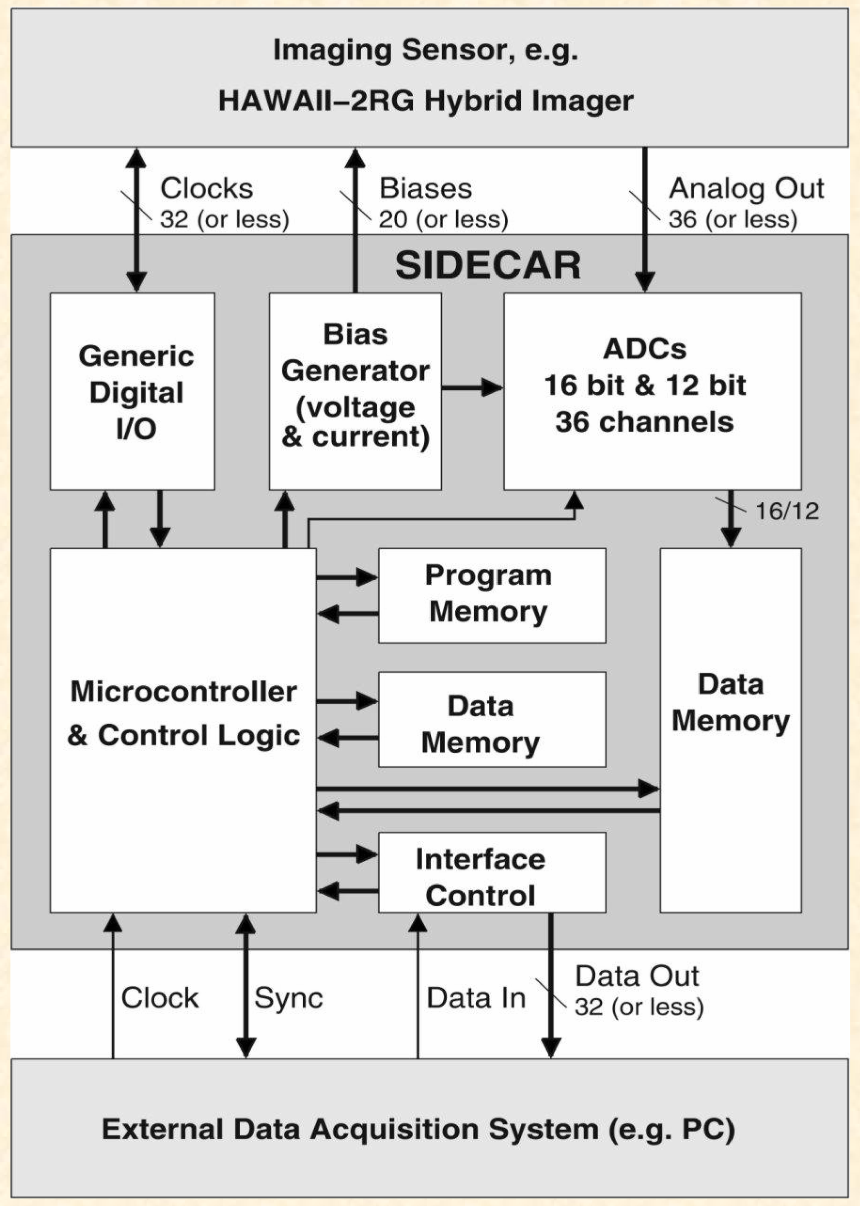


Figure 5: Block diagram of the SIDECAR

The SIDECAR ASIC: focal plane electronics on a single chip
Markus Loose *et al.*, Proc. SPIE Int. Soc. Opt. Eng. 5904, 59040V (2005) *(10 pages)*