Introduction

This document provides a short introduction to Local Bus signals and protocols for PLX's line of PCI Bus-Mastering IO Accelerator products, including PCI 9054, PCI 9056, PCI 9656 and PEX 8311 devices. This covers just the basics of the local bus for first-time designers. For complete descriptions of local bus behavior, refer to the data sheet for your specific part.

Note that PCI 9030, PCI 9050, and PCI9052 devices have similar local bus signaling, but these devices only support accesses from PCI to local bus. There are other notable differences as well that are not covered here. This tutorial covers primarily the PCI 9054, PCI 9056, PCI 9656, and PEX 8311 devices.

Terms Used in this Document

Local Bus Master	The agent on the bus that drives the address onto the local bus and drives the data bus for a write access or latches the data for a read access.
Local Bus Slave	The agent on the bus that receives and successfully decodes the local address, and responds by either driving data for a read access or latching data for a write access.
Local Bus Access	A transaction on the local bus beginning with an Address Phase, and ending with one or more Data Phases. These will be explained later in the document.

Transaction Types

There are three main types of transfers that are supported by the PCI 9xxx/PEX 8311 bridge. These are Direct Slave, Direct Master, or DMA. A fourth type of local bus transaction, Local Configuration Register access, involves only the Local bus, targeting internal registers. These are explained below.

Direct Slave

A Direct Slave transfer originates on PCI/PCI Express bus, and targets a range of PCI addresses that are mapped to a device on the local bus. When PCI 9xxx/PEX 8311 receives a read or write request from PCI/PCIe that is mapped to the local bus, it requests mastership of the local bus from an external arbiter. Once granted, PCI 9xxx/PEX 8311 becomes the local bus master and performs the access to the local bus. For a PCI/PCIe write, PCI 9xxx/PEX 8311 forwards PCI/PCIe write data directly to local bus. For a PCI/PCIe read, PCI 9xxx/PEX 8311 performs a read access to a local slave, and then returns the read data to the PCI requester.

Direct Master

A Direct Master transfer originates on local bus, and targets a range of PCI addresses that are mapped to a device on the PCI/PCI Express bus. For these types of accesses, PCI 9xxx/PEX 8311 is the local bus slave. When PCI 9xxx/PEX 8311 decodes a read access with an address mapped to PCI space, it generates a PCI/PCIe read request. Read data returned on PCI are then forwarded to the local bus master. When PCI 9xxx/PEX 8311 decodes a write access with an address mapped to PCI space, it generates a PCI/PCIe write and forwards write data directly.

DMA

A DMA transfer originates within PCI 9xxx/PEX 8311 from one of two on-board DMA channels. For a Local-to-PCI/PCIe DMA transfer, PCI 9xxx/PEX 8311 becomes the local bus master, and reads data from the targeted local slave. Read data from local bus are then written to PCI/PCIe by the PCI 9xxx/PEX 8311. For a PCI/PCIe-to-Local DMA transfer, PCI 9xxx/PEX 8311 generates read requests to PCI/PCIe. When read data are received from PCI/PCIe, PCI 9xxx/PEX 8311 acquires mastership of the local bus and forwards PCI/PCIe read data to the local slave in the form of a local bus write access.

Local Bus Configuration Register Access

Local Configuration Register accesses are very similar to Direct Master accesses, except that a special chip-select signal, CCS# is asserted. For this type of access, PCI 9xxx/PEX 8311 is a local slave. By driving CCS# low, the local bus master indicates that the local address indexes one of the internal configuration registers within PCI 9xxx/PEX 8311. As such, CCS# accesses do not cross the bridge to PCI/PCIe - they target internal registers only.

Local Bus Modes

PCI 9xxx / PEX 8311 devices support three different local bus protocols, or modes. The specific mode used is hard-wired for a specific design and selected via MODE[1:0] strapping signals as listed below.

Table 1. Local Bus MODE selection straps

MODE[1:0] Strapping Balls (L = Low / H = High)	Bus Mode
LL	**C Mode**
LH	**J Mode**
HL	Reserved
HH	**M Mode**

C Mode

C Mode is a synchronous, non-multiplexed bus with separate address and data busses, and is signal-compatible with Intel i960 processors. Bit ordering is little-endian (bit 31 is MSB).

J Mode

J Mode is a synchronous, multiplexed address/data bus that is signal compatible with Intel i960 Jx processor, Freescale PowerPC 401, and others. Bit ordering is little-endian (bit 31 is MSB). The control signals, timing and protocol for C and J modes are almost identical; the main difference being C-Mode is non-multiplexed and J-Mode is multiplexed.

M Mode

M Mode is a synchronous, non-multiplexed bus with separate address and data, and is signal-compatible with Motorola MPC 850, MPC 860, or PowerQUICC processors. Bit ordering for these processors is big-endian (bit 0 is MSB). Because PCI/PCI Express is little-endian by design, PCI 9xxx/PEX 8311 has the ability to perform endian conversion for accesses passing from PCI/PCIe to local bus and vice-versa. Endian conversion is complex and beyond the scope of this document. For details, refer to the data sheet for your specific part.

C/J-Mode Local Bus Signals

Local bus signals specific to C/J Modes are listed in table 2 below. There are additional signals in this group that are not listed here (BTERM#, BREQi, etc.), whose functions are beyond the scope of this document. See the data sheet for your specific part for details on these signals.

Table 2. C/J Mode Local Bus Signals

Signal	Description
LCLK	**Local Bus Clock** This is the primary clock for the Local bus. All local bus signals and accesses are synchronous with the rising edge of this clock. (exception is ALE). LCLK must be toggling and stable prior to the end of reset and running at all times after the end of reset.
LHOLD	**Local Bus Hold** Asserted by the PCI 9xxx/PEX 8311 to request access to Local Bus for Direct Slave (from PCI/PCIe) or DMA (internally generated) transfers. This signal is routed to an external local bus arbiter.
LHOLDA	**Local Bus Hold Acknowledge** Asserted by an external local bus arbiter to grant access to the local bus. When asserted, PCI 9xxx/ PEX 8311 can begin a local bus access as a local master. For simple local bus applications where PCI 9xxx/PEX 8311 is the only local bus master, LHOLDA can be connected directly to LHOLD and pulled to ground through a resistor.
ADS#	**Address Strobe** This signal is output for Direct Slave or DMA accesses to local bus (when PCI 9xxx / PEX 8311 is the local master), and input for Direct Master or Local Configuration Register accesses. When asserted, ADS# signals the start of a local bus access, and qualifies the address on LA[31:2] (C-Mode) or LAD[31:2] (J-Mode).
ALE	**Address Latch Enable (J-Mode)** This signal is asserted by the local master during the Address Phase of a local bus access. It can be used to latch the valid address from the LAD bus. If ADS# is used for latching local address, then ALE need not be used.
LW/R#	**Local Write / Read Select** Indicates the direction of transfer on the local bus. High indicates the local master is writing to the local slave. Low indicates the local master is reading the local slave.
BLAST#	**Burst Last** This signal is asserted by the local master to signal the final Data phase of a local bus access.
READY#	**Ready** This signal is asserted by the local slave to indicate that valid read data is on the bus and ready to be latched by the master or that it is ready to latch write data at the next rising clock edge. The local slave can insert wait states between address and data phases or between successive data phases by driving READY# high. Local slaves must drive READY# high at the end of a local bus access. The READY# handshake is optional for each of the local spaces, enabled by local configuration registers (LBRDn[6], DMAMODEn[6]).

Signal	Description
WAIT#	**Wait** This signal is optionally asserted by the local master to insert programmed wait states between Address and Data phases, or between successive Data phases within a burst accesses. The local bus slave must monitor WAIT# and not transfer data when WAIT# is asserted, regardless of whether the local slave is asserting READY#. When PCI 9xxx/PEX 8311 is the local master (Direct Slave or DMA transaction), WAIT# is an output, with the number of wait states programmed by way of a local configuration register, LBRDn[5:2] or DMAMODEn[5:2]. When PCI 9xxx/PEX 8311 is the local slave (Direct Master transaction), WAIT# is an input, and may be optionally driven by the local master to insert wait states.
LBE[3:0]#	**Local Bus Byte Enables** Encoded, based on the bus data-width configuration, as follows: **32-Bit Bus** The four Byte Enables indicate which of the four bytes are valid during a Data cycle: LBE3# Byte Enable 3 – LD[31:24] LBE2# Byte Enable 2 – LD[23:16] LBE1# Byte Enable 1 – LD[15:8] LBE0# Byte Enable 0 – LD[7:0] **16-Bit Bus** LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively: LBE3# Byte High Enable (BHE#) – LD[15:8] LBE2# *not used* LBE1# Address bit 1 (LA1) LBE0# Byte Low Enable (BLE#) – LD[7:0] **8-Bit Bus** LBE[1:0]# are encoded to provide LA[1:0], respectively: LBE3# *not used* LBE2# *not used* LBE1# Address bit 1 (LA1) LBE0# Address bit 0 (LA0)
LA[31:2]	**Local Address bus (C-Mode)** (LA31:2 are also valid in J-Mode, though these signals would not be bused to other J-Mode devices)
LD[31:0]	**Local Data bus (C-Mode)**
LAD[31:0]	**Local Multiplexed Address/Data bus (J-Mode)**
CCS#	**Configuration Chip Select** CCS# is asserted by a local master (CPU) when accessing PCI 9xxx / PEX 8311 internal configuration registers. Configuration accesses are identical to Direct Master accesses, except that CCS# is asserted. CCS# should only be driven during a local Configuration access. It must remain high at all other times.

C-Mode Direct Slave / DMA Read Access Example

Figure 1 illustrates a C-Mode Direct Slave or DMA read access from a local slave device. In this access PCI 9xxx / PEX 8311 requests ownership of the bus as a local master. Once the local arbiter grants the local bus, the PCI 9xxx / PEX 8311 drives local bus control lines and performs the access.
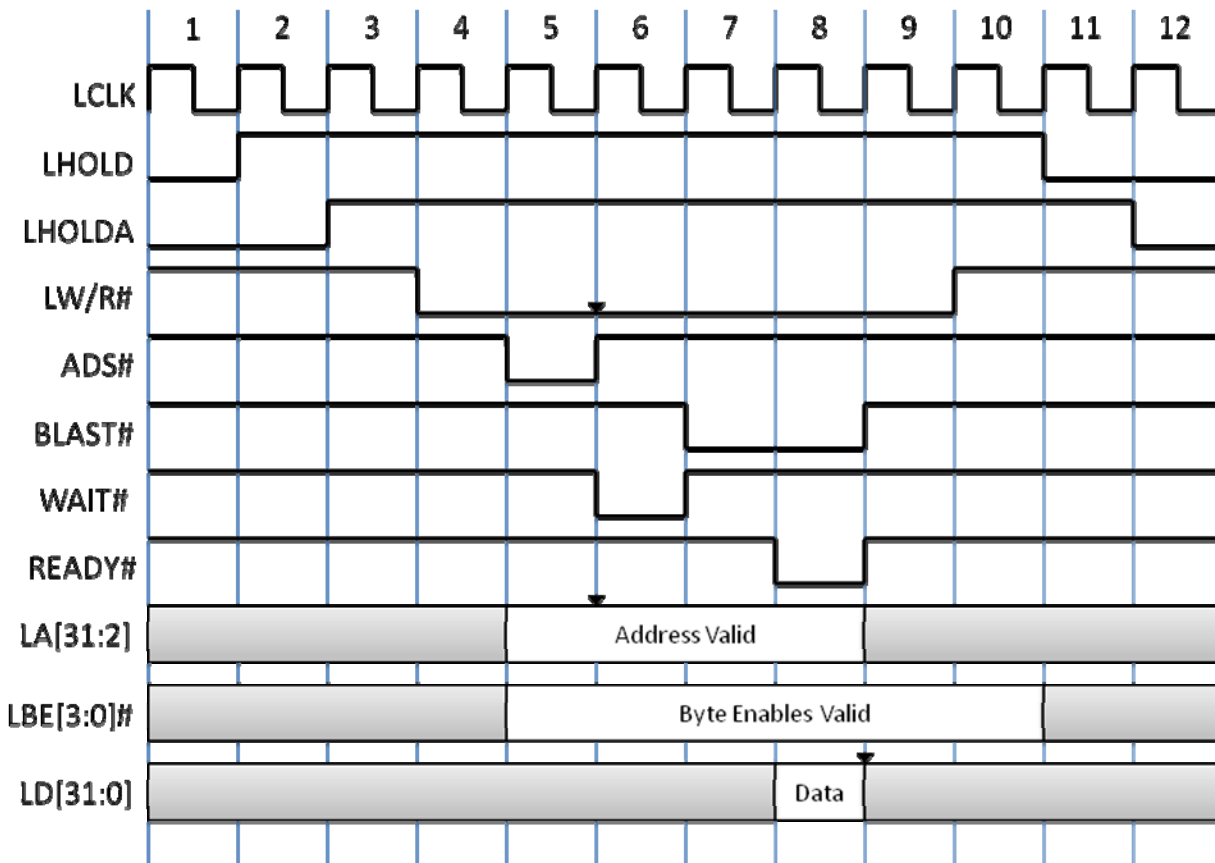
Figure 1. C-Mode Direct Slave or DMA Single DWord Read from Local Slave (32-bit local bus)
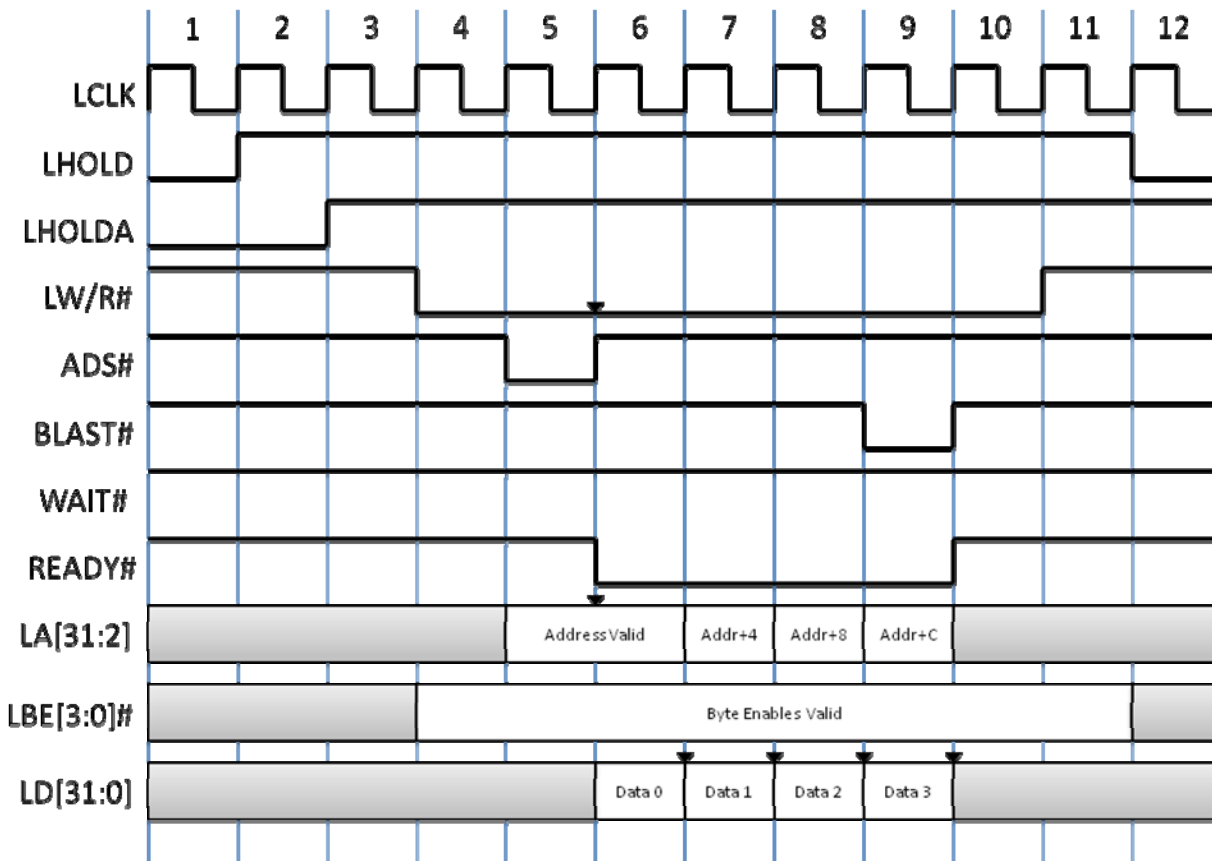
Cycle-by-cycle notes for Figure 1 are listed below:

1. Local bus is IDLE. LHOLD/LHOLDA are not asserted, LW/R#, ADS#, BLAST#, LBE[3:0]#, LA, LD lines are hi-z (inputs).
2. PCI 9xxx/PEX 8311 requests local bus mastership from the external arbiter by asserting LHOLD.
3. External arbiter grants local bus to PCI 9xxx/PEX 8311 by asserting LHOLDA. For simple applications where PCI 9xxx/PEX 8311 is the only local master, LHOLD can be directly tied to LHOLDA, with both signals pulled low by a pull-down. This will shorten the arbitration time.
4. LW/R# may be driven out one LCLK before the Address Phase. LW/R# low indicates a read from the local slave. LW/R# is not valid until the Address Phase.
5. **Address Phase.** The local master (PCI 9xxx/PEX 8311) drives the local address onto LA[31:2] and asserts ADS# to signal the start of the local bus access. LA[31:2] and LW/R# are valid at the next

rising edge of LCLK. Local bus slaves decode the address at this time to determine whether or not the access is addressed to them.

6. **Master-inserted wait state.** This is an optional state(s) programmed by way of a local bus configuration register (LBRDn[5:2] or DMAMODEn[5:2] = 0001b), and signaled by WAIT# assertion on the local bus. Local slaves must monitor WAIT# when used, and not transfer data when it is asserted.

7. **Slave-inserted wait state.** When the READY# handshake is enabled via local configuration registers (LBRDn[6] or DMAMODEn[6]), PCI 9xxx/PEX 8311 will not latch read data until READY# is sampled low. The local slave can then insert any number of additional wait states by holding READY# high.

8. **Data Phase.** The local slave drives one DWord of read data onto LD[31:0] and qualifies the data by asserting READY# low. PCI 9xxx/PEX 8311 latches the data at the next rising edge of LCLK. PCI 9xxx/PEX 8311 asserts BLAST# to signal the local slave that this is the final data phase of the local bus access.

9. Local slave must drive READY# high following the access.

10. LW/R# is released.

11. LHOLD# is de-asserted, PCI 9xxx/PEX 8311 releases local bus (hi-z).

12. Idle.

C-Mode Direct Slave / DMA Burst Read Example

Figure 2 illustrates a Direct Slave or DMA burst read of 4 DWords from a local slave, with no wait states.

Figure 2. C-Mode Burst Read of 4 DWords from a 32-bit local slave.
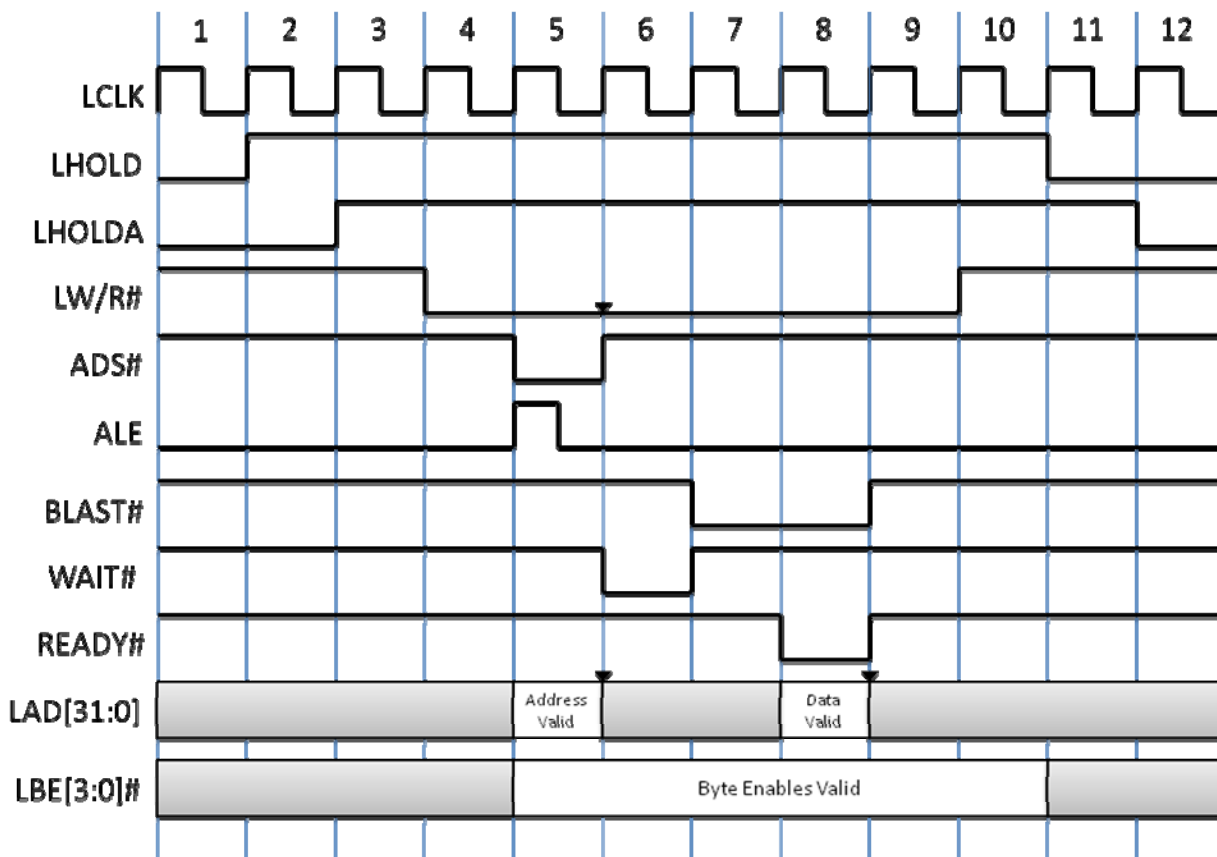
Cycle-by-cycle notes for Figure 2 are listed below:

1. Local bus is IDLE. LHOLD/LHOLDA are not asserted, LW/R#, ADS#, BLAST#, LBE[3:0]#, LA, LD lines are hi-z (inputs).
2. PCI 9xxx/PEX 8311 requests local bus mastership from the external arbiter by asserting LHOLD.
3. External arbiter grants local bus to PCI 9xxx/PEX 8311 by asserting LHOLDA.
4. LW/R# and LBE[3:0]# may be driven out one LCLK before the Address Phase. LW/R# and LBE[3:0]# are not valid until the Address Phase.
5. **Address Phase.** PCI 9xxx/PEX 8311 drives address onto LA[31:2] and asserts ADS# to indicate the start of the local bus access. Local slaves sample LA[31:2] and LW/R# at the next rising edge of LCLK and decode the address at this time to determine whether or not the access is addressed to them.
6. **Data Phase 0.** The local slave drives the first DWord of read data onto LD[31:0] and qualifies the data by asserting READY# low. PCI 9xxx/PEX 8311 latches the data at the next rising edge of LCLK.
7. **Data Phase 1.** Second DW of data are transferred. Address on LA increments.
8. **Data Phase 2.** Third DW of data are transferred. LA increments.

9. **Data Phase 3.** Last DW of the transfer. LA increments. PCI 9xxx/PEX 8311 asserts BLAST# to signal the local slave that this is the final data phase of the local bus access.
10. Local slave must drive READY# high at the end of the access.
11. PCI 9xxx/PEX 8311 drives LW/R# high before releasing the bus.
12. LHOLD de-asserted. Local bus is released (hi-z).

J-Mode Direct Slave / DMA Read Access Example

Figure 3 below illustrates a PCI 9xxx/PEX 8311 in J-Mode performing a Direct Slave or DMA read from a local slave.

Figure 3. J-Mode Direct Slave or DMA single DWord read from a 32- bit local slave

In Figure 3, cycle-by-cycle notes are listed below:
1. Local bus is IDLE. LHOLD/LHOLDA are not asserted, LW/R#, ADS#, BLAST#, LBE[3:0]#, LAD lines are hi-z (inputs).
2. PCI 9xxx/PEX 8311 requests local bus mastership from the external arbiter by asserting LHOLD.
3. External arbiter grants local bus to PCI 9xxx/PEX 8311 by asserting LHOLDA.
4. LW/R# may be driven out one LCLK before the Address Phase. LW/R# and LBE[3:0]# are not valid until the Address Phase.

5. **Address Phase**. PCI 9xxx/PEX 8311drives local address onto LAD[31:0] and asserts ADS# low to indicate the start of the local bus access. ALE also pulses high for approximately ½ LCLK time, as shown. Either ADS# or ALE can be used to latch the address from LAD bus. Local bus slaves decode the address at this time to determine whether the access is addressed to them.

6. **Master-inserted wait state.** This is an optional state(s) programmed by way of a local bus configuration register (LBRDn[5:2], DMAMODEn[5:2]), and signaled by WAIT# assertion on the local bus. Local slaves must monitor WAIT# when used, and not transfer data when it is asserted.

7. **Slave-inserted wait state.** When the READY# handshake is enabled via local configuration registers (LBRDn[6] or DMAMODEn[6]), PCI 9xxx/PEX 8311 will not latch read data until READY# is sampled low. The local slave can then insert any number of additional wait states by holding READY# high.

8. **Data Phase.** The local slave drives the read data onto the LAD[31:0] bus and qualifies it by driving READY# low. PCI 9xxx/PEX 8311 latches the read data at the next rising edge of LCLK. BLAST# asserted at this time indicates that this is the final data phase of the access.

9. The local slave must drive READY# high at the end of the local bus access.

10. PCI 9xxx/PEX 8311 drives LW/R# high before releasing the bus.

11. LHOLD de-asserted. Local bus is released (hi-z).

12. Idle.

J-Mode Direct Slave / DMA Burst Read Example

Figure 4 shows PCI 9xxx/PEX 8311 in J-Mode performing a Direct Slave or DMA read from a 32-bit local slave. In this example, there are no wait states inserted, either programmed (WAIT# low) or by the local slave (READY# high). Note also that for this example, PCI 9xxx/PEX 8311 is the only local master, and LHOLDA is directly connected to LHOLD, thus minimizing the number of overhead clocks. When performing DMA transfers, PEX 9xxx/PEX 8311, with its deep FIFOs can sustain very long bursts, nearly saturating local bus bandwidth.
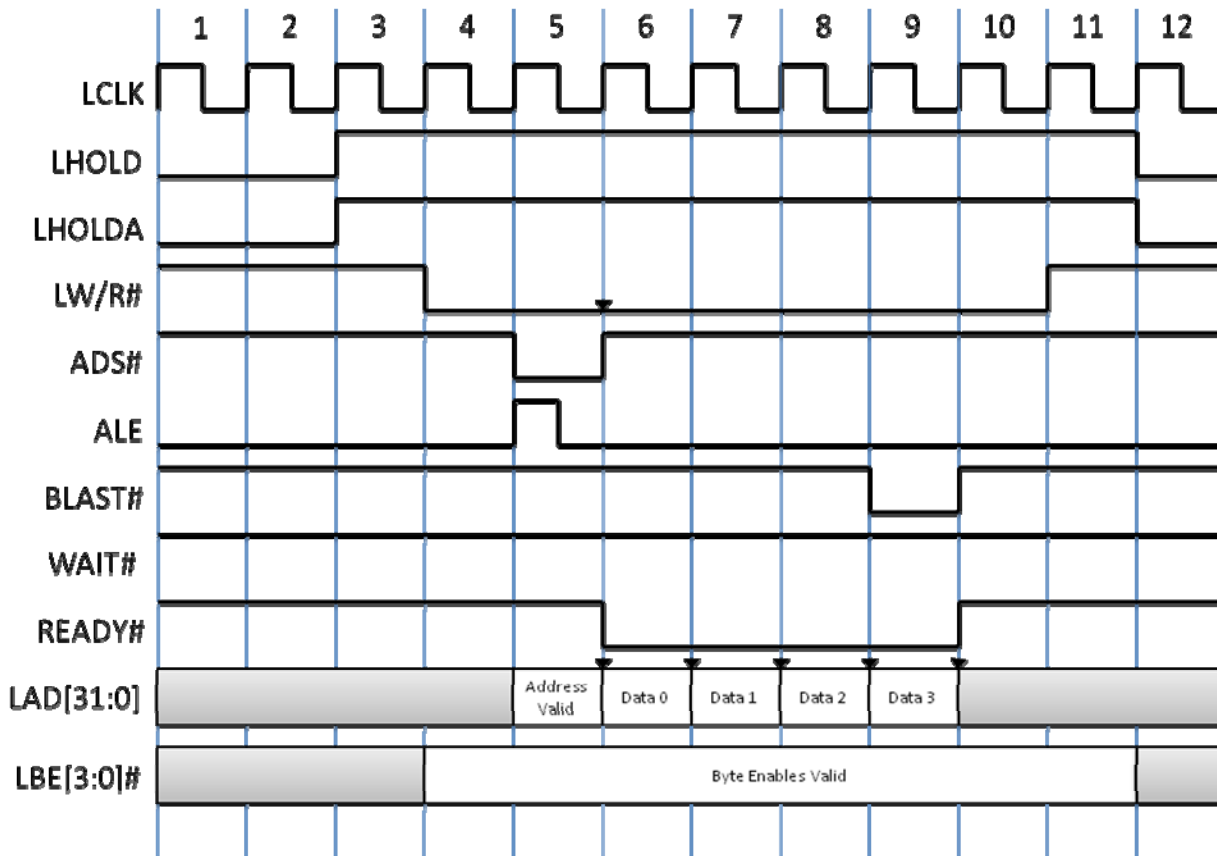
Figure 4. Direct Slave or DMA burst read of 4 DWords from a local slave.

Notes for Figure 4 are as follows:

1. Idle
2. Idle
3. PCI 9xxx/PEX 8311 asserts LHOLD to acquire mastership of the local bus. Since there are no other local masters in this example, LHOLDA is directly tied to LHOLD.
4. LW/R# and LBE[3:0]# may be driven out one LCLK before the Address Phase. LW/R# and LBE[3:0] are not valid until the Address Phase.
5. **Address Phase.** PCI 9xxx/PEX 8311drives local address onto LAD[31:0] and asserts ADS# low to indicate the start of the local bus access. ALE also pulses high for approximately ½ clocks. Either

ADS# or ALE can be used to latch local address from the LAD bus. Local bus slaves decode the address at this time to determine whether the access is addressed to them.

6. **Data Phase 0.** The local slave drives the first DWord of read data onto the LAD[31:0] bus and qualifies it by driving READY# low. PCI 9xxx/PEX 8311 latches data at the next rising edge of LCLK.
7. **Data Phase 1.** Second DW of data is transferred. The local slave is responsible for incrementing the address latched during the address phase.
8. **Data Phase 2.** Third DW of data is transferred.
9. **Data Phase 3.** Last DW of the transfer. PCI 9xxx/PEX 8311 asserts BLAST# to signal this is the final data phase of the local bus access.
10. Local slaves must drive READY# high at the end of the access.
11. LW/R# is driven high before hi-z.
12. LHOLD de-asserted. Local bus is released (hi-z).

M-Mode Local Bus Signals

Local bus signals specific to M-Mode local bus are listed in table 2 below. There are additional signals in this group that are not listed here whose functions are beyond the scope of this document. See the data sheet for your specific part for details on these signals.

Table 3. M-Mode Local Bus Signals

Signal	Description
LCLK	**Local Bus Clock** This is the primary clock for the Local bus. All local bus signals and accesses are synchronous with the rising edge of this clock.
BR#	**Bus Request** Asserted by PCI 9xxx/PEX 8311 to request mastership of local bus for Direct Slave or DMA access to a local bus slave device.
BG#	**Bus Grant** Asserted by the external local bus arbiter to grant mastership of the local bus to PCI 9xxx/PEX 8311 for Direct Slave or DMA accesses to local bus. If PCI 9xxx/PEX 8311 is the only local bus master, this signal can be pulled low always.
BB#	**Bus Busy** Asserted by PCI 9xxx/PEX 8311 to signal that a Direct Slave or DMA access is about to begin and that PCI 9xxx/PEX 8311 is driving local bus control and address lines.
TS#	**Address Strobe** This signal is output for Direct Slave or DMA accesses to local bus (when PCI 9xxx / PEX 8311 is the local master), and input for Direct Master or Local Configuration Register accesses. When asserted, ADS# signals the start of a local bus access, and qualifies the address on LA[0:31].
RD/WR#	**Local Read / Write Select** Indicates the direction of transfer on the local bus. Low indicates the local master is writing to the local slave. High indicates the local master is reading the local slave.
BURST#	**Burst** This signal is asserted by the local master during the Address phase to indicate that multiple

Signal	Description
	data phases will follow.
BDIP#	**Burst Data In Progress** The local master asserts BDIP# for all Data phases of the burst except the last one. When the local slave samples BDIP# high, it knows that the current data phase is the last one for that local access.
TA#	**Transfer Acknowledge** This signal is asserted by the local slave to indicate that valid read data is on the bus and ready to be latched by the master or that it is ready to latch write data at the next rising clock edge. The local slave can insert wait states between address and data phases or between successive data phases by driving TA# high. Local slaves must drive TA# high at the end of a local bus access. The TA# handshake is optional for each of the local spaces, enabled by local configuration registers (LBRDn[6], DMAMODEn[6]).
WAIT#	**WAIT** This signal is optionally asserted by the local master to insert programmed wait states between Address and Data phases, or between successive Data phases within a burst accesses. The local bus slave must monitor WAIT# and not transfer data when WAIT# is asserted, regardless of whether the local slave is asserting READY#. When PCI 9xxx/PEX 8311 is the local master (Direct Slave or DMA transaction), WAIT# is an output, with the number of wait states programmed by way of a local configuration register, LBRDn[5:2] or DMAMODEn[5:2]. When PCI 9xxx/PEX 8311 is the local slave (Direct Master transaction), WAIT# is an input, and may be optionally driven by the local master to insert wait states.
TSIZ[0:1]	**Transfer Size** TSIZ[0:1] are encoded together with LA[30:31] to enable individual byte lanes during the Data phase of a local bus access. For the examples provided in this document, it is assumed that all local accesses are aligned, 32-bit accesses. For details on TSIZ[1:0] encoding for non-aligned accesses or for 8-, 16-bit local bus widths, refer to the data sheet for your specific part.
LA[0:31]	**Local Address bus**
LD[0:31]	**Local Data bus**
CCS#	**Configuration Chip Select** CCS# is asserted by a local master (CPU) when accessing PCI 9xxx / PEX 8311 internal configuration registers. Configuration accesses are identical to Direct Master accesses, except that CCS# is asserted.

M-Mode Single DW Write Example

Figure 5 below shows PCI 9xxx/PEX 8311 in M-Mode performing a single DWord write (Direct Slave or DMA) to a local bus slave. In this example, there are two wait states inserted between address and data phases, one by the local master (PCI 9xxx/PEX 8311) and one by the local slave.
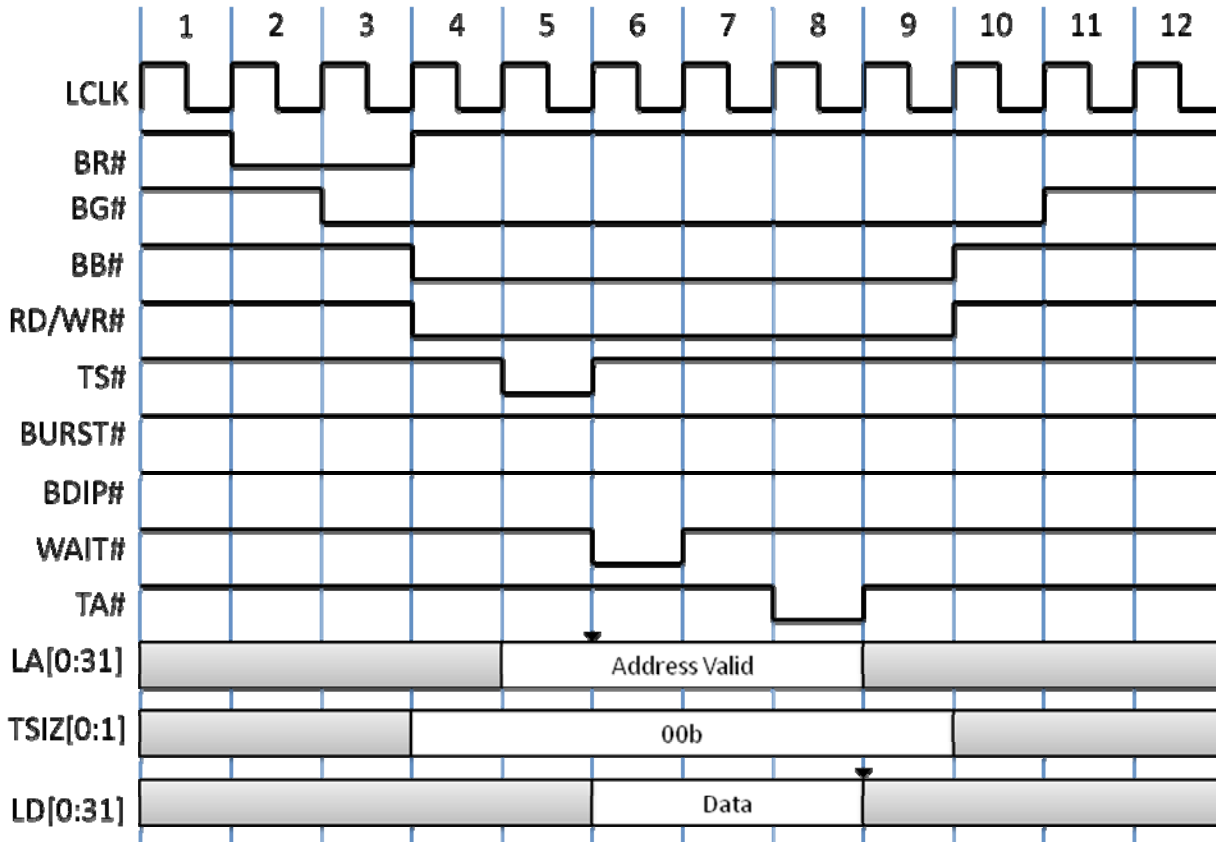
Figure 5. M-Mode Direct-Slave or DMA single DWord write to a 32-bit local slave

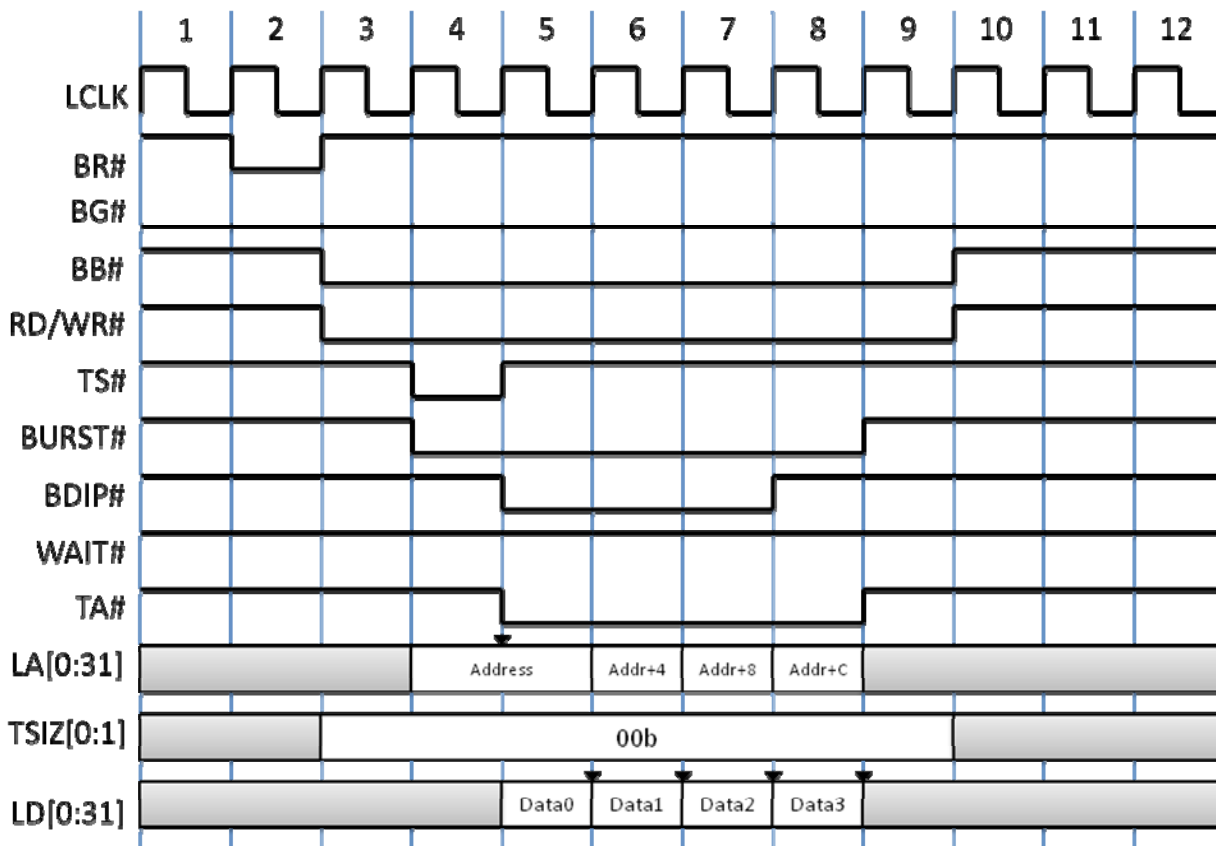Notes for Figure 5 are as follows:
1. Bus Idle (hi-z)
2. PCI 9xxx/PEX 8311 asserts BR# to request ownership of the local bus. BR# is routed to an external local bus arbiter (local CPU or FPGA).
3. External arbiter asserts BG#, granting ownership of the local bus to PCI 9xxx/PEX 8311.
4. PCI 9xxx/PEX 8311 becomes a local master by asserting BB#. Upon sensing BG# low, BR# is de-asserted.
5. **Address Phase.** PCI 9xxx/PEX 8311 drives local address onto LA[0:31] and asserts TS# to signal the start of the local bus access. Local slaves decode LA[31:0] at this time to determine whether the access is addressed to them.
6. **Master-inserted wait state.** This is an optional state(s) programmed by way of a local bus configuration register (LBRDn[5:2] or DMAMODEn[5:2] = 0001b). PCI 9xxx/PEX 8311 signals the

wait state by asserting WAIT# low. Local slaves must monitor WAIT# when used, and not transfer data when it is asserted.

7. **Slave-inserted wait state.** When the TA# handshake is enabled by way of local configuration registers (LBRDn[6] or DMAMODEn[6]), PCI 9xxx/PEX 8311 will not transfer data until TA# is asserted by the local slave. When TA# is enabled, the local slave can insert additional wait states by holding TA# high. In such cases, the local access will not complete until TA# is asserted.

8. **Data Phase.** The local slave signals its readiness to latch write data by driving TA# low. The local slave then latches write data from the LD bus at the next rising edge of LCLK.

9. Local slaves must drive TA# high at the end of the local access.

10. PCI 9xxx/PEX 8311 drives BB# high and releases the bus (hi-z).

M-Mode Burst Write Example

In Figure 6, below, PCI 9xxx/PEX 8311 in M-Mode is shown performing a DMA burst write of four DWords to a 32-bit local slave. In this example, PCI 9xxx/PEX 8311 is the only local bus master in the system. In this case, no external arbiter is needed, and BG# can be pulled low always. (BR# is not used). Also, in this example, there are no wait states. Four DWords of data are transferred on consecutive clocks.

Figure 6. M-Mode DMA burst write of 4 DWords to a 32-bit local slave

Notes for Figure 6 are as follows:

1. Idle
2. PCI 9xxx/PEX 8311 asserts BR# to request ownership of the local bus. This is meaningless for this example since PCI 9xxx/PEX 8311 is the only local master in the system and BG# is low always.
3. PCI 9xxx/PEX 8311 asserts BB# and begins to drive RD/WR#, TSIZ[0:1].
4. **Address Phase.** PCI 9xxx/PEX 8311 drives local address onto LA[0:31] and asserts TS# to signal the start of the local bus access. Local slaves decode LA[31:0] at this time to determine whether the access is addressed to them. Also, BURST# is asserted by PCI 9xxx/PEX 8311 to indicate that a burst access is to follow.
5. **Data Phase 0.** PCI 9xxx/PEX 8311drives the first DWord of write data onto LD[0:31] and asserts BDIP# to signal a burst access in progress. The local slave asserts TA# to signal its readiness to accept the data (no wait states). Local slave latches the first DWord at the next rising edge of LCLK.
6. **Data Phase 1.** PCI 9xxx/PEX 8311increments LA[0:31] by 4 and drives the second DWord of the burst onto LD[0:31]. The local slave latches the data at the next rising edge of LCLK.
7. **Data Phase 2.** PCI 9xxx/PEX 8311increments LA[0:31] by 4 and drives the third DWord of the burst onto LD[0:31]. The local slave latches data at the next rising edge of LCLK. PCI 9xxx/PEX 8311 de-asserts BDIP# to signal that the next data phase will be the last one for this access.
8. **Data Phase 3.** PCI 9xxx/PEX 8311increments LA[0:31] by 4 and drives the third DWord of the burst onto LD[0:31]. The local slave latches data at the next rising edge of LCLK.
9. PCI 9xxx/PEX 8311 drives BURST# high at the end of the local access. The local slave must also drive TA# high at this time.
10. PCI 9xxx/PEX 8311 de-asserts BB# and releases the local bus (hi-z).