Space Qualification and Performance Results of the SIDECAR ASIC

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ABSTRACT

The SIDECAR ASIC is a fully integrated FPA controller system-on-a-chip. Compared to conventional control electronics, it requires significantly less power, less space and less weight. The SIDECAR ASIC, which can operate at ambient and cryogenic temperatures, is currently being space-qualified for integration in the science instruments of the James Webb Space Telescope (JWST). This paper gives an overview of the SIDECAR architecture and its supporting drive electronics. It describes the JWST flight configuration including the custom packaging approach. Test results obtained as part of the space qualification effort are presented. CDS noise of the ASIC itself amounts to less than 25 μV for full 2K x 2K data frames. The noise reduces to less than 6 μV for up-the-ramp-sampling with 88 frames. Based on the existing qualification results and a number of additional tests in the next few months, NASA Technology Readiness Level 6 (TRL6) will be demonstrated by August 2006.

Keywords: ASIC, SIDECAR, Focal Plane Electronics, JWST, HAWAII-2RG, A/D Conversion

1. INTRODUCTION

About 4 years ago, the development of a new generation of controller for CMOS-based focal plane arrays was initiated at Rockwell Scientific. Instead of making boards filled with discrete electronics components like ADCs, DACs, FPGAs and memories, the idea was to integrate all circuits required for the operation of an FPA onto a single micro-chip. First prototypes of the new controller concept were available about a year later in form of an application specific integrated circuit (ASIC), named SIDECAR™ for System for Image Digitization, Enhancement, Control And Retrieval. After improving upon a few initial shortfalls, full functionality and excellent performance results of the SIDECAR ASIC have been measured and reported (Loose et al. [1]). As a consequence, NASA has decided that all near-infrared instruments of the James Webb Space Telescope (JWST) replace their conventional discrete electronics approach with the SIDECAR ASIC (Rauscher et al. [2]).

This paper focuses on the latest developments and results as part of the JWST space qualification program. First, a general overview of the SIDECAR ASIC architecture is given, illustrating the various building blocks and functions. Subsequently, the two main packaging concepts are presented, one specifically designed for the JWST application, the other one being a more generic multi-functional approach. In this context, the paper also describes a custom USB-based controller system to connect and operate the SIDECAR ASIC with a standard PC. Finally, a number of measurement results are presented demonstrating the noise performance of the ASIC at a temperature of 37K.

In addition to meeting the functional requirements, the SIDECAR ASIC has to also undergo a number of mechanical and electrical stress tests to meet NASA's Technology Readiness Level 6 (TRL6). This includes vibration and shock as well as burn-in and long-term reliability testing. Since the SIDECAR will operate at cryogenic temperatures, the typical burn-in and reliability tests for room temperature components are not fully applicable. Therefore, in addition to the

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regular burn-in at an elevated temperature, the parts will also see a 1000 hour "freeze-in" at the operating temperature of T=37K. Long-term reliability will be verified by running several parts for >10,000 hours, also at operating temperature. These tests are in preparation and will be completed by August 2006, with the exception of the 10,000 hour lifetime test.

2. SIDECAR OVERVIEW

The SIDECAR ASIC is a fully programmable control and digitization system for analog image sensors. It is designed to operate from room temperature all the way down to cryogenic temperatures as low as 30 K. It is optimized for use with analog CMOS-based detector arrays that require biases, clocks and power supplies in the range from 0 to 3.3V. Figure 1 shows a block diagram of a typical SIDECAR-driven detector system and a microscope photograph of the chip itself. The top block in the block diagram represents the FPA, which is connected to the SIDECAR (center block) via many analog and digital wires. At the bottom of the SIDECAR block, only digital wires go to the external data acquisition system. Due to the immunity of the digital signal transmission, which can be LVDS or LVCMOS, the acquisition system can be located several meters away from the SIDECAR ASIC.

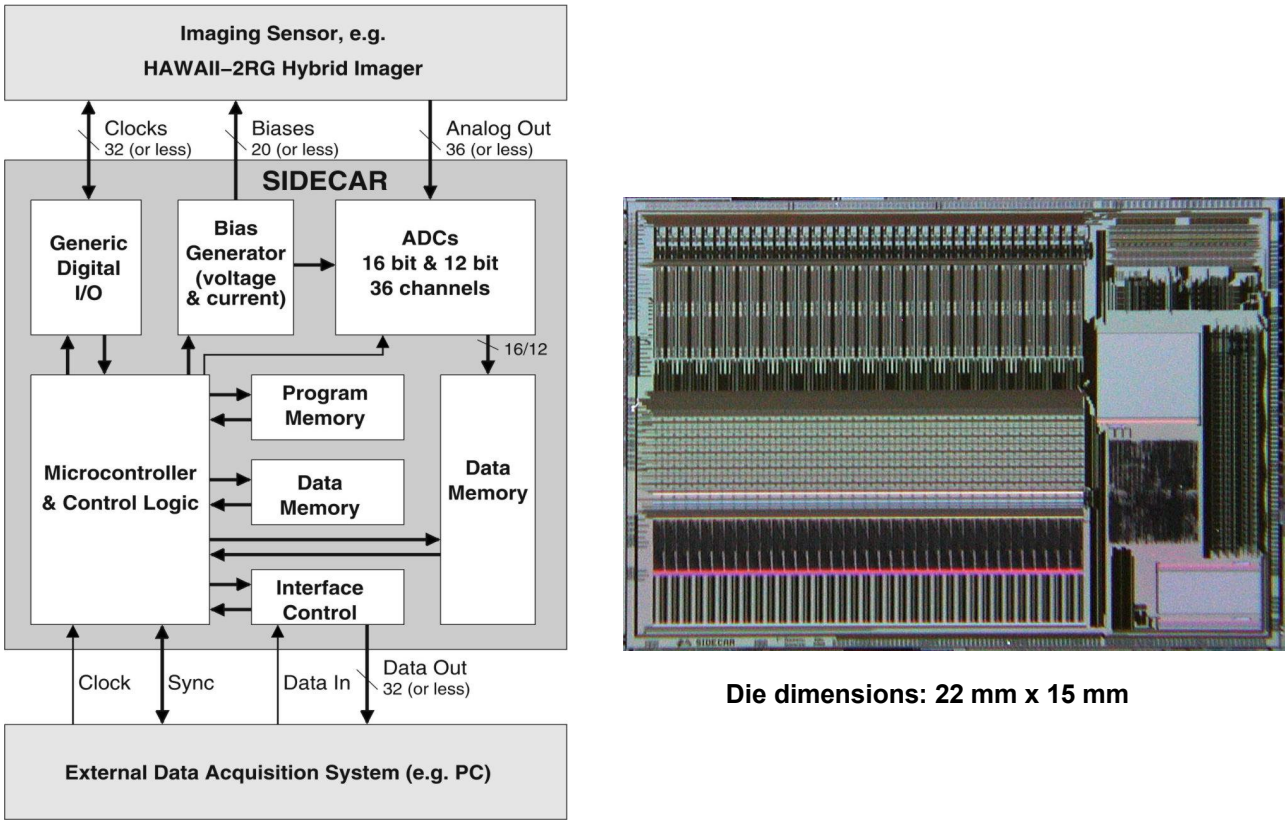

Figure 1: Block diagram (left) and die micrograph (right) of the SIDECAR ASIC.

The basic SIDECAR architecture, as shown in the diagram, can be divided into the following major blocks: generic digital I/O, bias generator, A/D converter, digital control and timing generation (micro-controller), data and program memory, and digital data interface.

The analog bias generator consists of 20 independent channels, each of which is composed of a 10-bit digital-to-analog converter and an output buffer with adjustable driver strength. Each channel can be used as a programmable current source from 0.1µA to 25mA and a programmable voltage source covering the range from 0V to 3.3V. For reading out

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the analog detector signals, the SIDECAR provides 36 analog input channels. Each channel can be digitized by on-chip ADCs offering 16-bit resolution at sample rates up to 500 kHz and 12-bit resolution at sample rates up to 10 MHz.

A fully programmable and application optimized micro-controller is responsible for the overall SIDECAR control and for generating the specific timing patterns of the image sensor clocks. A total of 32 digital I/O channels can be individually adjusted for driver strength and signal direction. Additional on-chip memory linked to an array processor with 36 channels permits simple data processing functions like pixel averaging or data sorting. Finally, serial and parallel data interfaces are implemented to read the digitized pixel values and to program the ASIC. The data interface can be operated at speeds up to 80 Mbits per line in single data rate mode (one bit per clock cycle) with a maximum bus width of 24 signals. Therefore, the maximum data bandwidth is about 1.9 Gbit/s and corresponds to 32 analog detector channels digitized at 5 MHz with 12 bit resolution.

Table 1 summarizes the main SIDECAR ASIC properties. Only a small fraction of the capabilities are used for JWST, e.g. only 4 of the analog inputs are required. However, the extra number of channels provides significant redundancy in case of a failure in orbit. Since the extra channels can be all powered down if not in use, they do not cause any increase in power consumption over the normal consumption in 4-channel JWST mode.

Table 1: Summary of the SIDECAR ASIC properties

Die Dimension	22 x 14.5 mm²
Technology	0.25 µm CMOS
Analog Input	36 independent channels, fully differential
Preamplifiers	Programmable gain (-3 to 27 dB) and bandwidth
16 bit ADCs	Up to 500 kHz sample rate (1 mW / channel at 100 kHz)
12 bit ADCs	Up to 10 MHz sample rate (10 mW / channel at 5 MHz)
Bias Outputs	20 output channels, selectable voltage or current DACs
Digital I/O	24 channels (CMOS), 16 channels (LVDS) fully programmable
Micro-controller	16 bit RISC, low power, excellent arithmetic capabilities
Program Memory	16 kwords (16 bit / word)
Data Memory (µC)	8 kwords (16 bit / word)
Data Memory (ADC)	36 kwords (24 bit / word)
Array-processor	Adding & multiplying and DMA control per ADC channel
Digital Interface	LVDS or CMOS, custom serial protocol, up to 32 parallel lines
Operating Temperature range	30 K – 300 K
Radiation	Complete design is single event upset protected

3. PACKAGING

3.1. Generic Full-Function Package

The SIDECAR ASIC has a total of 365 pads which are distributed around its perimeter. A significant portion is dedicated to power and provides a low impedance connection to the various on-chip power and ground nets. All other pads are used as either digital I/Os (data interface, clocks), analog I/Os (biases, preamp inputs) or reference voltage pads for external capacitive filtering. A 337-pin custom package has been developed that provides access to all SIDECAR pads. The reduction in pin count compared to the SIDECAR pad count results from combining multiple power pads on the same package pin. The package is available in two flavors: a micro-PGA version and an LGA version. Each of them

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supports the full functionality of the SIDECAR ASIC. For cryogenic operation, however, the LGA is preferred because it can much better compensate for thermally induced stress between the package and the mounting socket.

Both package flavors are based on a ceramic chip carrier with inserted copper-tungsten core providing excellent thermal contact to the ASIC die. The package size is about 36mm x 36mm. Figure 2 shows a photograph of the SIDECAR ASIC packaged in the micro-PGA and the LGA package. The LGA package is currently used and recommended for all ground-based astronomy applications and is included as part of the SIDECAR development kit. The development board comprising one SIDECAR ASIC (socket in the center of the board) and a number of test points and LEDs can be seen in the right half of Figure 2.

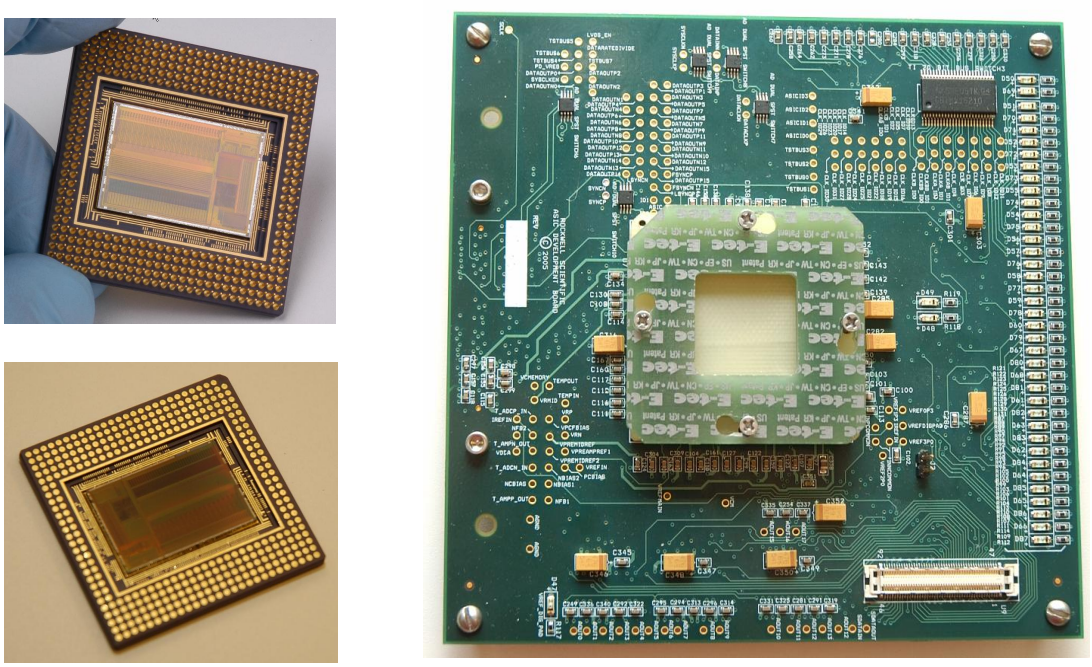

Figure 2: SIDECAR ASIC packaged in a PGA package (top left) and an LGA package (bottom left) with 337 pins each, and the development board with the SIDECAR ASIC socket (right).

3.2. JWST Flight Package

To guarantee clean supply voltages and to provide noise filtering on the analog bias and reference signals, the SIDECAR ASIC requires a number of bypass capacitors close to the chip. In case of the generic package approach presented in the previous section, the capacitors are placed on the board next to the SIDECAR socket. For JWST, however, a different packaging approach was chosen to be able to retrofit the existing instrument designs with the SIDECAR. Here, the SIDECAR die is directly mounted and wire-bonded to a ceramic circuit board that provides sufficient room for all passive components. The ceramic board has a very high thermal conductivity and ensures optimum heat sinking. Figure 3 shows a photograph of the JWST SIDECAR package, with and without the surrounding metal box. The pictures are scaled approximately 1-to-1. The package also comprises a bottom and a top lid, which have been left off in the picture for the sake of clarity.

On either end of the ceramic board, a 37-pin micro-D connector links the external cables to the corresponding signals of the SIDECAR ASIC. One connector handles the mixed-mode interface to the HAWAII-2RG detector and includes clocks, bias voltages and 6 analog input channels. The other connector provides access to the digital interface and the power supplies. It also includes the signals for the on-board temperature sensor and the optional heater resistors. The metal enclosure provides electrical as well as optical shielding and protects the SIDECAR die against mechanical damage.

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The SIDECAR assembly will be located close to the detectors within each JWST science instrument and will operate at 37K. The control electronics, on the other hand, will be located several meters away and will operate under room temperature conditions. Therefore, a special thermally resistive cable needs to bridge the two regions by keeping the thermal load a small as possible. The disadvantage of such cables is the high electrical resistance and the poor shielding characteristics. Clean separation into various power domains and custom low-current LVDS signals for the digital communication have been employed to achieve reliable low noise operation under the given conditions.

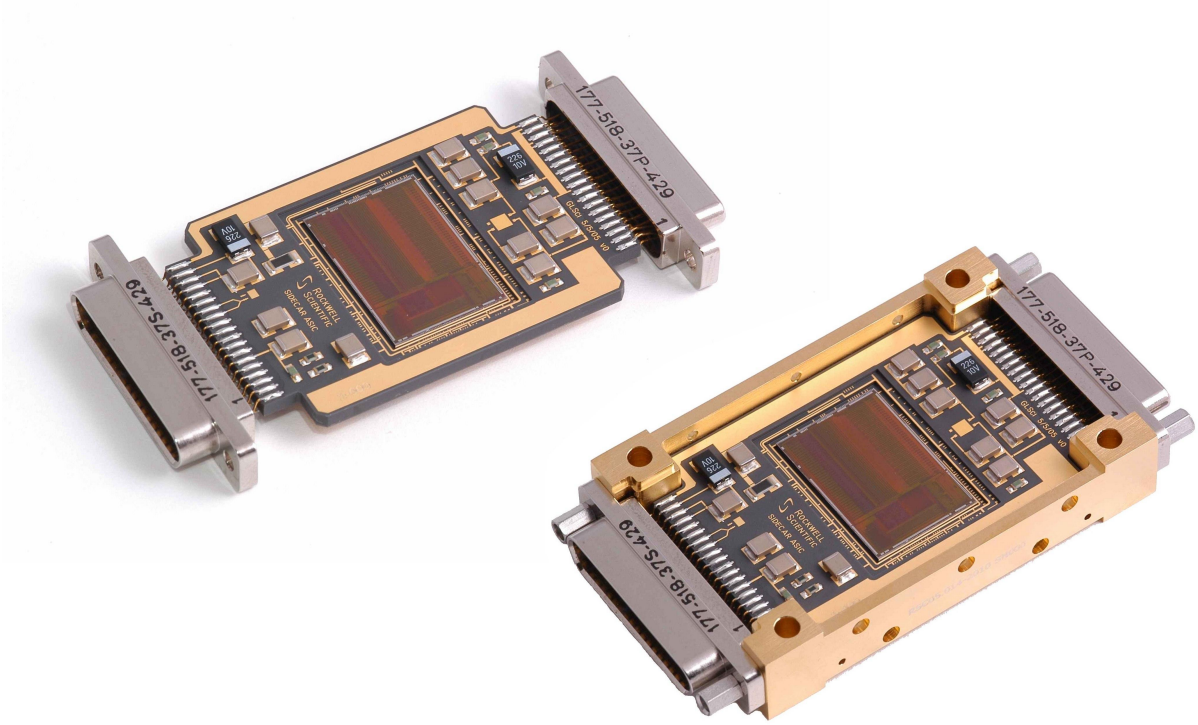

Figure 3: JWST flight package: Ceramic circuit board with ASIC die and passive components, shown without and with metal housing, dimensions are about 74 x 38 x 10.4 mm^3.

4. SIDECAR DRIVE ELECTRONICS

In general, operation of the SIDECAR ASIC merely requires power and communication via the digital interface. However, for the sake of making the SIDECAR suitable for low-power cryogenic space applications, a custom interface protocol has been implemented that is not compatible with any other interface standard. Thus, connecting the ASIC to an acquisition host like a personal computer necessitates the use of an intermediate logic component to translate the SIDECAR protocol. A custom controller card, called JADE2 for JWST ASIC Drive Electronics Version 2, has been built for this purpose and is used for all of the JWST qualification testing. Figure 4 shows the block diagram and figure 5 a photograph of the JADE2 card.

The JADE2 controller card connects directly to a PC through its USB 2.0 port. In addition to the digital data transfer, the USB connector also provides 5V power. For low noise or high current applications, a separate power connector is available. The JADE2 board generates a total of 24 programmable voltage sources to drive multiple independent SIDECAR ASICs. Each voltage source is equipped with a voltage and current read-back circuit to measure power consumption and to monitor the operation. A Spartan-3 FPGA handles the protocol translations from the SIDECAR to

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the USB controller chip. It also interfaces to 32 MByte of embedded memory which allows intermediate storage of up to four 2K x 2K image frames. A 140-pin high density connector enables a variety of SIDECAR system configurations.

Each SIDECAR ASIC can be configured to have a unique 4-bit identification number. By this means, up to 16 SIDECARs can be controlled by the same clock and data lines. Furthermore, the JADE2 card can operate up to 4 separate banks of clock lines, data lines and power supplies. Altogether, up to 64 SIDECARs can be driven with a single JADE2 card. The ultimate limitation besides the number of SIDECAR ASICs, however, is given by the maximum data bandwidth on the USB port. Although theoretically capable of transmitting over 50 Mbytes/s, only about half of that has been demonstrated so far. Assuming one 2k x 2k detector per SIDECAR running in 4 output mode at 100 kHz pixel rate, the available 25 Mbyte bandwidth is sufficient to operate 32 SIDECAR ASICs in parallel on one JADE2 card.

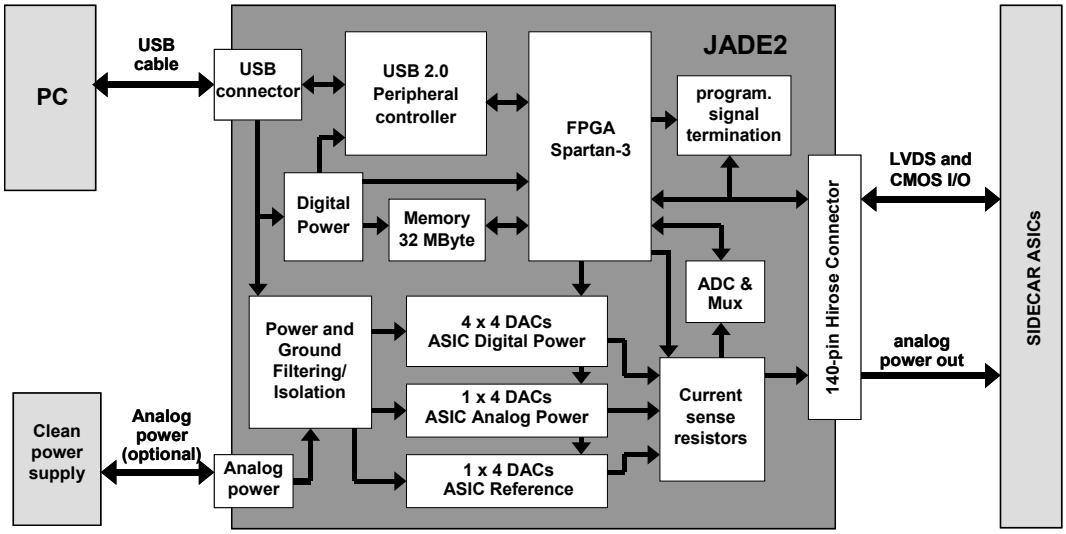

Figure 4: Block diagram of the JADE2 controller card for the SIDECAR ASIC.

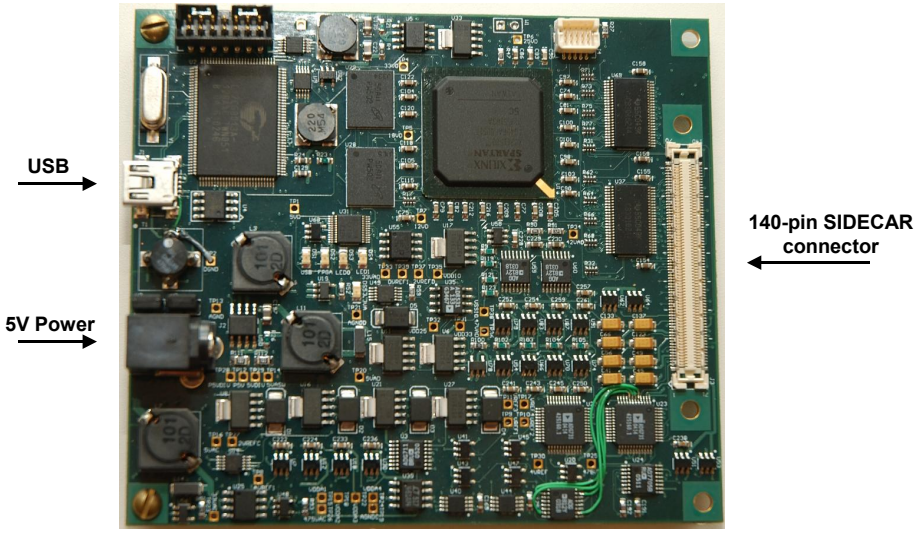

Figure 5: JADE2 controller card for operation of up to 64 SIDECAR ASICs in parallel, dimensions are 10 x 9 cm^2.

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5. MEASUREMENT RESULTS

Room temperature and cryogenic measurement results of the SIDECAR ASIC's performance and functionality have been published before (Loose et al. [1] and Wong et al. [3]). However, these results were obtained in a non-flight configuration using the 337-pin PGA package. Since then, the JWST specific SIDECAR package has been developed, and it needed to be demonstrated that the SIDECAR ASIC can meet the requirements in a space-like configuration. A custom cryostat was built to hold 4 flight-packaged SIDECARs and 4 HAWAII-2RG detectors at the same time. Cooling down and testing 4 parts simultaneously is essential for achieving the necessary production throughput. All four ASICs are controlled and powered by one JADE2 card which is located outside the cryostat.

The performance characterization of the flight packaged SIDECAR ASIC focuses on the noise, and those are the results presented in the next sections. All other parameters like power consumption or linearity are not expected to depend on the packaging concept and have not yet been re-characterized in the flight configuration. They will be verified as part of the production control and verification process on each individual SIDECAR ASIC, however. Table 2 briefly summarizes the previously obtained results for analog performance and power consumption (JWST mode of 4 ADCs at 100 kHz sampling rate each).

Table 2. Analog performance and power consumption in a JWST-like configuration

Parameter	Measurement Result
Preamplifier noise at T = 37K	12 µV (input referred at 27 dB Gain)
12-bit ADC linearity	DNL < ± 0.3 LSB, INL < ± 0.8 LSB
16-bit ADC linearity	DNL < ± 0.4 LSB, INL < ± 2.3 LSB
Power consumption	< 10.5 mW (4 ADCs, 100 kHz sample rate)

5.1. SIDECAR ASIC Full Frame Noise Performance

Detectors and SIDECAR ASICs will be delivered separately and independently to the JWST science instruments. For that reason, they have to be characterized independently, and each SIDECAR has to be able to work with any detector. Consequently, an upper limit needed to be set for the noise contribution of the ASIC itself. Since the SIDECAR ASIC, to first order, is just an electronic circuit that does not care about electrons or conversion gain, the noise requirement was established as a voltage noise as opposed to an electron noise: 26.5 µV for a single CDS frame.

The noise is measured by shorting the differential pre-amplifier inputs and digitizing full 2K x 2K images in a typical JWST configuration. This means, running four 16-bit ADCs in parallel, each digitizing 2048 rows times 64 pixels at 100 ksample/s. The gain of the pre-amplifier is set to 21 dB in order to correctly map the detector output swing to the input range of the ADC. Unfortunately, this gain setting is lower than the maximum gain of 27 dB, and therefore results in an increased noise compared to the lowest noise possible. The reason is that the ADC noise contribution becomes more pronounced the lower the gain of the pre-amplifier. All measurements have been carried out at T=37K.

Figure 6 shows the noise map and the noise histogram of a full 2K x 2K CDS frame, digitized by the SIDECAR ASIC with its preamp inputs shorted. The histogram as well as the map are shown in ADUs, with a conversion factor of 4.2µV/ADU. The data has been obtained by taking a total of 20 CDS frames, and calculating the standard deviation for each pixel throughout the 20 frames. This approach is commonly referred to as the temporal method. The histogram yields a median noise of just under 6 ADUs or 25µV, thus meeting the JWST CDS noise requirements of 26.5 µV.

A second noise number, which can be compared to the total noise requirement of the NIRSpec instrument, has been measured. Basically, 88 frames are being read non-destructively, and then arranged in 22 groups of 4. The average of the 4 frames in each group is calculated, and a least-square fit is performed on the 22 average frames to calculate the slope of the ramp. NIRSpec expects this so-called multi-accum 22-4 sampling scheme to achieve a total system noise of less than 6 electrons. The identical scheme has been applied to ramp data of the SIDECAR ASIC with shorted inputs, and the results can be seen in figure 7. Assuming a detector conversion gain of 4.2 µV/e-, the noise contribution of the

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SIDECAR ASIC is less than 1.2 e-, or about 2% of the total noise budget of 6e- if added in quadrature. The noise was determined by taking 20 ramps and calculating the slope variation from ramp to ramp for each pixel.

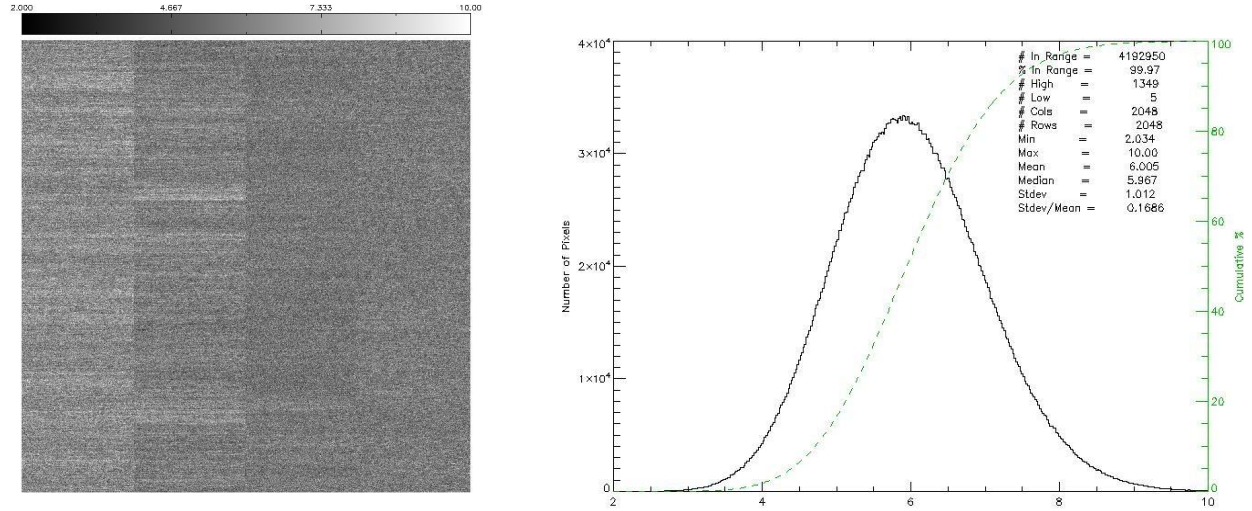

Figure 6. Noise map and histogram (single CDS) of the SIDECAR ASIC with shorted pre-amplifier inputs.

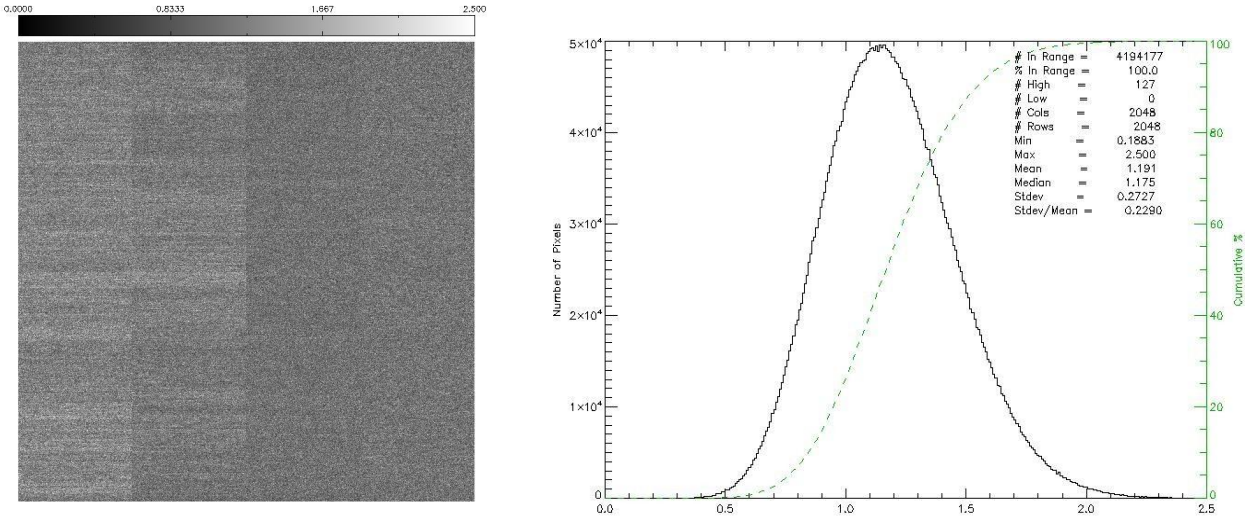

Figure 7. Noise map and histogram (NIRSpec's multiaccum 22-4) of the SIDECAR ASIC with shorted pre-amplifier inputs.

5.2. Noise Performance of HAWAII-2RG with SIDECAR ASIC

In addition to the SIDECAR ASIC performance itself, a complete system comprising an engineering grade HAWAII-2RG hybrid FPA with a 2.5µm cutoff HgCdTe detector and a flight-packaged SIDECAR has been tested. The measurements were performed at the nominal JWST operating temperature of 37K. At that temperature, dark current is at 0.01 e-/s, and the dark current shot noise for a 1000s exposure is small enough to not dominate the total noise. Figure 8 contains a single read frame, clearly showing the HAWAII-2RG picture frame effect around the perimeter. This effect cancels out completely in a simple CDS frame, but allows easy verification of the correct operation of the acquisition system. Also, the four parallel output channels can be seen, showing a slight variation in offset from channel to channel (4 vertical bars, each 512 pixels wide and 2048 pixels tall).

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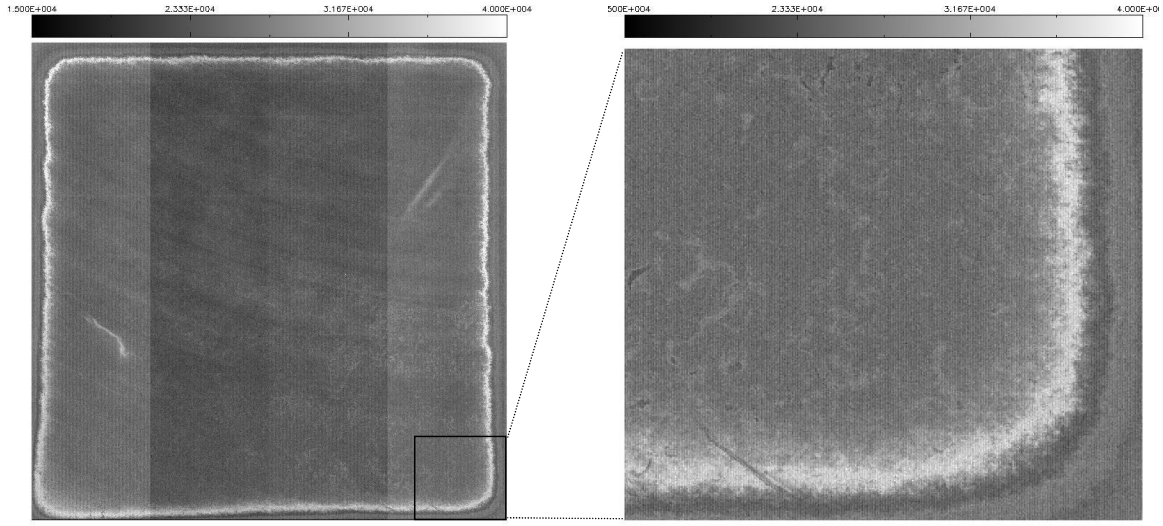

Figure 8: Image map and magnified cutout of a HAWAII-2RG hybrid with 2.5µm cutoff, controlled by the SIDECAR ASIC at 37K.

The following image maps and histograms show noise data in ADUs with a conversion factor of 4.2µV/ADU. The typical conversion gain of a HgCdTe detector hybridized to a HAWAII-2RG and measured with the variance method (noise^2) is somewhere between 3 and 4µV/e-, sometimes even above 4µV/e-. Taking the effect of the interpixel capacitance into account, which causes a systematic underestimation of the shot noise, the true conversion gain is about 20% higher (Finger et al. [4] and Moore et al. [5]). The actual conversion gain therefore spreads from about 3.6µV to over 4.8µV/e-, and the mid-level value is at 4.2µV/e-. In other words, the following plots can be directly interpreted in units of electrons rather than ADUs, with 1 ADU = 1 electron.

Figure 9 shows the noise results of a single CDS frame, calculated by looking at the standard deviation of each pixel through a set of 20 CDS frames. A median noise of about 21e- has been measured, which is typical for these types of engineering devices. Some detector defects are apparent in the upper left region, and higher noise is observed in the upper right field. The bright line in the middle from top to bottom is caused by incomplete settling of the first pixel and can be eliminated by allowing slightly more settling time at the beginning of a row.

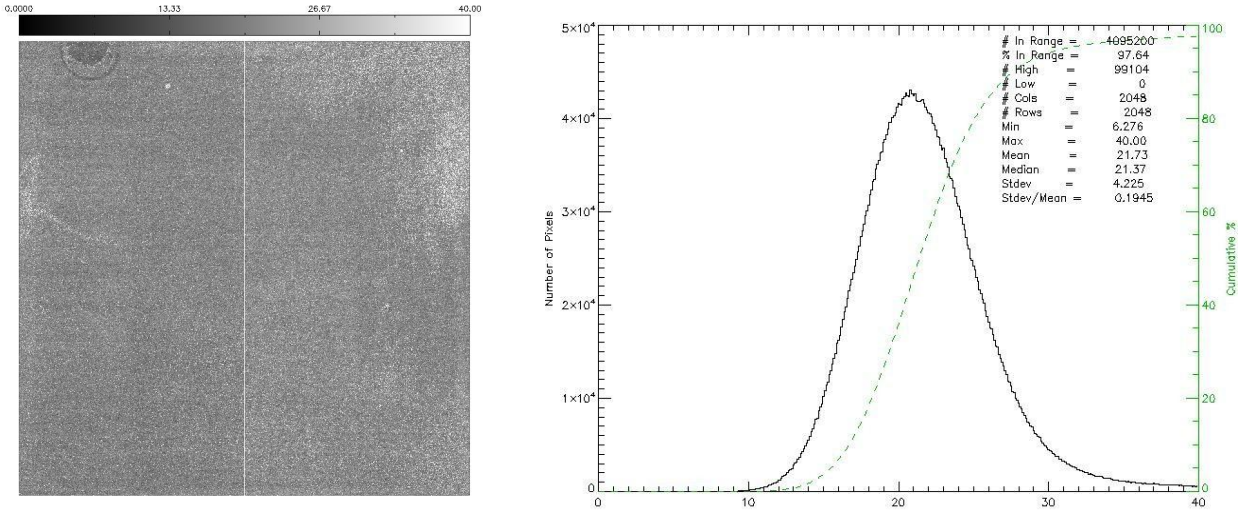

Figure 9. Noise map and histogram (single CDS) of a HAWAII-2RG hybrid with 2.5µm cutoff, controlled by the SIDECAR ASIC.

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The important performance requirements for any of JWST the detector subsystems are not given as a CDS noise number, but as a total noise after 1000s sampling up-the-ramp using a special instrument specific reduction scheme. For instance, NIRCam collects 48 frames, divided into 6 groups with 8 frames. This scheme has been applied to a data set of 20 ramps which have been collected with the same SIDECAR and detector system as the CDS frames before. The results are shown in figure 10, with a noise map on the left and the histogram on the right. Due to the longer integration time, a number of hot spots become visible, caused by hot pixels or cluster defects in the detector. In general, however, the noise has scaled down significantly, and the median noise is now below 7.8 electrons. This result meets the NIRCam requirement of 9 e-, despite the noisier characteristics of the engineering grade detector.

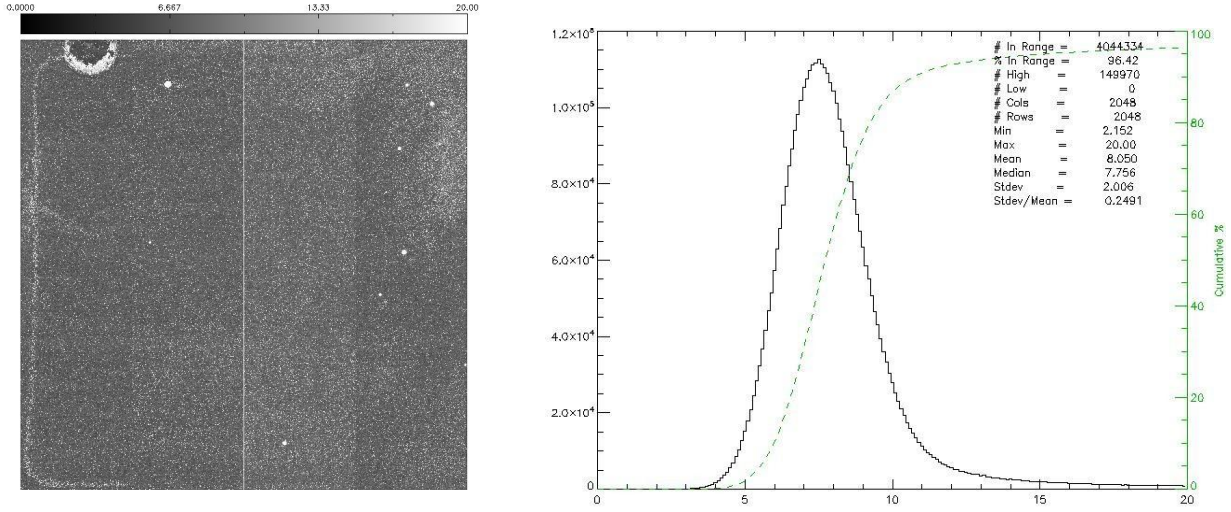

Figure 10. Noise map and histogram (NIRCam's multiaccum 6-8) of a HAWAII-2RG hybrid with 2.5µm cutoff, controlled by the SIDECAR ASIC.

An straight forward way of eliminating the detector noise from the equation is to examine the reference pixels. Their noise reflects only the system noise including the multiplexer, but is not affected by excess noise in the detector. Figure 11 contains a histogram of the reference pixels located in the outer four rows and columns of the HAWAII-2RG. As can be seen, the noise is reduced to 5.4e- for the NIRCAM sampling scheme.

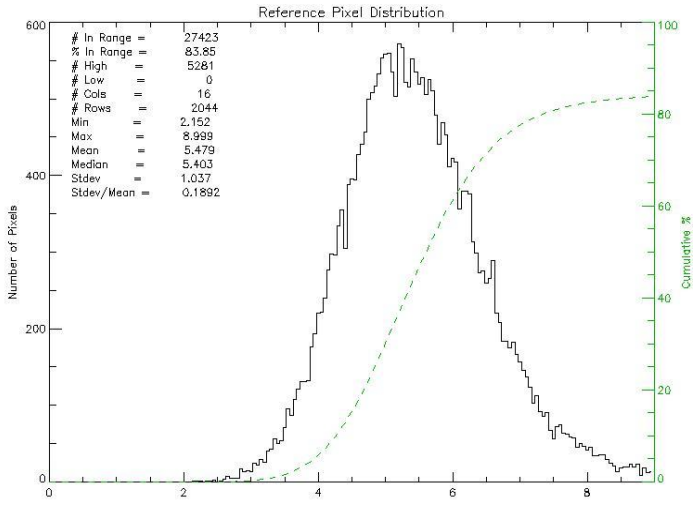

Figure 11. Reference pixel histogram (HAWAII-2RG) for the NIRCAM sampling scheme of 6 groups with 8 frames each.

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6. CONCLUSION

The SIDECAR ASIC is a fully integrated controller for analog focal plane arrays. It provides a large number of channels for clock generation, bias generation and analog to digital conversion, enabling the operation of multiple FPAs with a single SIDECAR. Two packaging concepts have been developed to date, one being a micro-PGA/LGA ceramic chip carrier with access to all SIDECAR options, the other one a flight package consisting of a ceramic circuit board, a number of passive filter components and two 37-pin connectors on either side. The flight package is restricted to the JWST operation of 4 parallel detector output channels.

The space qualification effort of the SIDECAR ASIC for the JWST program is progressing well. Several ASICs have been packaged in the flight configuration and tested for performance with and without a detector attached. At the nominal operating temperature of 37K, the noise of the ASIC itself has been measured to be 25 μV for a single CDS frame (21 dB preamp gain). Using a higher gain of 27 dB, CDS noise reduces to below 20 μV, but the dynamic range is reduced as well. Using multiple sampling as implemented for the NIRSpec instrument, the ASIC noise reduces to less than 6 μV. For a complete system of detector and SIDECAR ASIC, less than 8 electrons have been measured for the NIRCam sampling scheme. If taking into account only the reference pixels, the noise amounts to 5.4 electrons. All noise results meet the JWST requirements. Additional characterization and space qualification is continuing towards the goal of demonstrating TRL-6 in late summer of 2006.

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