Characterization of a ΣΔ-based CMOS monolithic detector

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ABSTRACT

This paper is a progress report of the design and characterization of a monolithic CMOS detector with an on-chip ΣΔ ADC. A brief description of the design and operation is given. Backside processing steps to allow for backside illumination are summarized. Current characterization results are given for pre- and post-thinned detectors. Characterization results include measurements of: gain photodiode capacitance, dark current, linearity, well depth, relative quantum efficiency, and read noise. Lastly, a detector re-design is described; and initial measurements of its photodiode capacitance and read noise are presented.

Key Words: ΣΔ, Sigma-Delta, Low Noise, CMOS Detector, On-chip ADC

1. INTRODUCTION

The probability of detecting a photon depends on numerous detector system properties, such as quantum efficiency, read noise, etc. A photon of sufficiently high energy will liberate photo-generated charge that migrates to a pixel collection node. In a direct readout architecture, such as that used in common CMOS detectors, this charge is converted to a voltage at the pixel and is then sensed at the detector output through a multiplexing circuit. In a CCD, the charge in the pixel is transferred across rows or columns and converted to a voltage at the output of the detector. In both CMOS and CCD architectures, the output voltage is usually amplified by external electronics. The tiny voltages in this circuit path are particularly vulnerable to externally-generated interference. Low detector noise is critical in photon-starved applications. One way to effectively reduce the noise susceptibility of a system is to digitize the analog voltage at a location that is as close to the pixel as possible. A digital output is immune to off-chip noise sources and can be operated at higher speeds. Also, the associated supporting electronics can be relatively simple, not needing specialized low noise amplification and digitization circuits.

This paper reports progress in developing a monolithic CMOS detector with an on-chip ΣΔ ADC[1]. The device design allows for back-side illumination and uses 3 transistor (3T) CMOS pixels multiplexed to an on-chip 1-bit ADC. The backside has been thinned at Jet Propulsion Laboratory (JPL), and devices will ultimately be delta-doped for enhanced short-wavelength response and better passivation[2,3,4,5]. The processes are discussed along with current process development. Characterization results are summarized, including results from pre- and post-thinned detectors. Characterization measurements include: gain, photodiode capacitance, dark current, linearity, well depth, relative quantum efficiency, and read noise. Finally, a re-design of the detector is described, and initial measurements of photodiode capacitance and read noise are reported.

2. DETECTOR DESIGN

2.1. CMOS Architecture

The current detector prototype is a 128x128 pixel monolithic Silicon (Si) array with 10 μm pixels. Each photodiode area is ~25 μm^2. The pixel circuit is a 3 transistor (3T) design. The detector was fabricated with the TSMC 0.35 μm CMOS process through the MOSIS service. The process includes a deposition of a ~8 μm thick epitaxial Si layer. The detectors are fabricated on ~3 mm^2 sections of silicon wafers which are diced. Some are packaged in a DIP 40-pin mount for

laboratory testing, while the rest are left as die for later processing. An image of a fabricated detector is shown in Figure 1. The active area is the grey square in the middle of the die.

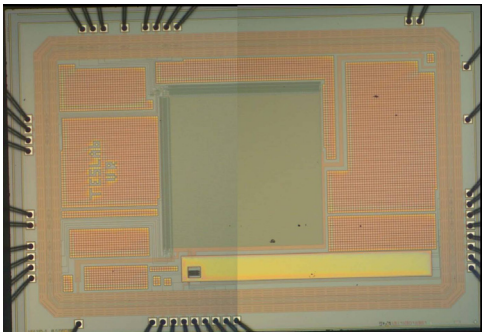

Figure 1. Picture of the ~3mm^2 detector die. The active area is the grey square in the center of the die. This prototype has 128 x 128 pixel array and 10 µm pixels with ~25 µm^2 photodiodes.

The readout integrated circuit (ROIC) design (see Figure 2) has row and column shift registers that multiplex the single output to the pixel array. The output is routed to the input of a comparator that is used for the ΣΔ readout. The output can also be connected to an output pad which provides direct access to the analog pixel signal, enabling detector characterization without using the ΣΔ readout.

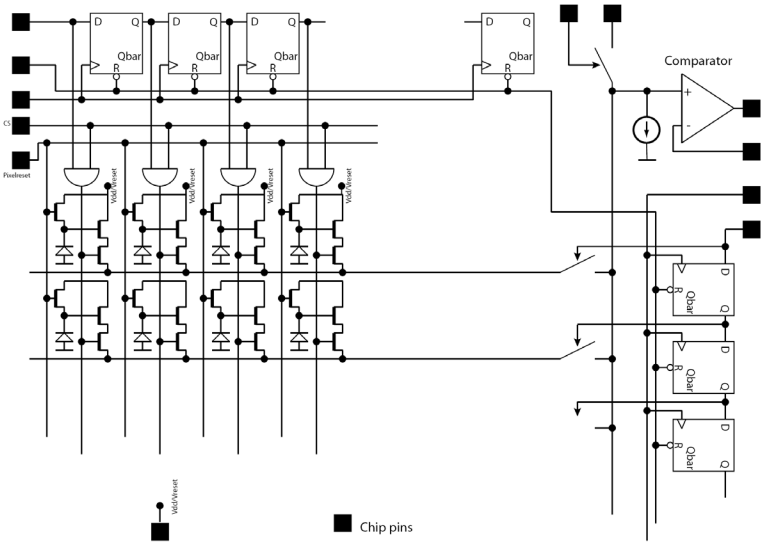

Figure 2. Partial Schematic of the detector design. The pixels uses a 3 transistor design which is multiplexed using row and column shift registers to a single output line. The output line connects to the input of an on-chip comparator used for the ΣΔ readout. The analog pixel signal can be routed off chip using a switch.

2.2. ΣΔ Design

The ΣΔ readout design for this chip is a modified form of a conventional 1st order ΣΔ converter[6,7]. Figure 3 shows a sequence of drawings that demonstrate its operation. In this design, a 3T photodiode circuit is used as the integrator. The photo-generated charge in the photodiode is converted to a voltage (V_{PD}) by the source follower FET. V_{PD} is compared to a threshold voltage (V_{Thresh}) by the comparator. In the current design, V_{Thresh} is supplied by an off-chip DAC. If V_{PD} is lower than V_{Thresh}, then the comparator output will be high, otherwise the output will remain low. Off-chip memory is

used to store the comparator output for processing. A high comparator output is counted as a digital 1 and a low comparator output is counted as a digital 0. The comparator output is used as a feedback to the off-chip DAC, which changes V_{Thresh}. V_{Thresh} is decremented when a 1 bit is received and incremented when a 0 bit is received. Figure 4 shows a simulation of how the ΣΔ ADC works. V_{PD} is constant which is equivalent to zero signal integration. The comparator is used to compare V_{PD} to V_{Thresh} and modulate V_{Thresh} based on the comparator output. This simulation shows that even with zero signal integration, a bit stream is still produced and will need to be subtracted from exposures in post processing. The fact that a bit stream is produced with zero signal means that in low flux environments a measurement of the integrated charge can be made. With oversampling, the bit stream accurately represents V_{PD}.

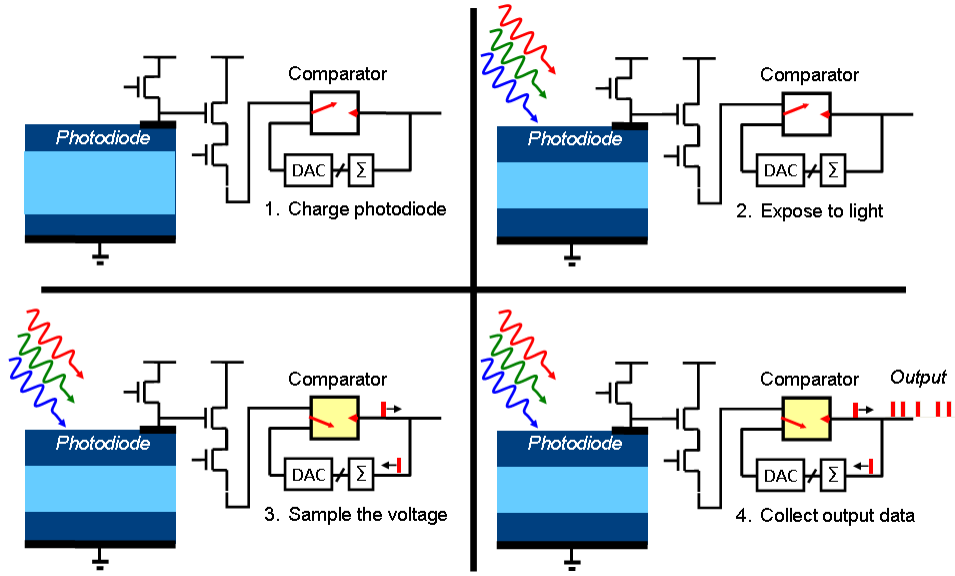

Figure 3. Analog-to-digital conversion process for ΣΔ ADC. The sequence proceeds from left to right and top to bottom.

The design allows for operation with different levels of flux because the feedback DAC step can be easily tuned based on the output bit stream. For high flux levels, V_{Thresh} can be modulated by a larger voltage step per comparator sample. In the case of low flux, the V_{Thresh} would be modulated by a smaller voltage step. In this way, the detector is only limited by the full well of the photodiode and the DAC range.

The ΣΔ readout design eliminates the need for correlated double sampling (CDS) that is commonly used to remove photodiode reset noise (kTC noise) and the transistor offsets in the pixel source followers. At the start of an exposure, all the photodiodes are reset to a starting bias voltage (V_{reset}). The row and column addressing connects a pixel to the output line. V_{Thresh} is set to a voltage near the reset level of V_{PD}. V_{thresh} is modulated by the ΣΔ readout and after a number of samples V_{Thresh} is within one modulation step of V_{PD} for that pixel. Then, the row and column addressing connects the next pixel to the output line and the process is repeated. This occurs for every pixel in the array. By ignoring the bits produced during this procedure, the kTC noise and the source follower transistor offsets are removed. Figure 5 shows a scope trace of the ΣΔ readout of a single pixel. The comparator bit stream at the beginning of the exposure is dominated by '1's because V_{Thresh} is set to a higher voltage than the reset level of V_{PD}. After a number of samples V_{Thresh} is reduced to match V_{PD} and the comparator output is no longer dominated by '1's.

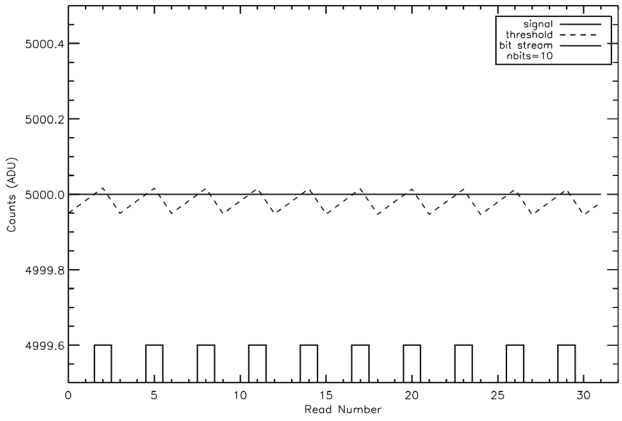

Figure 4. Simulated ΣΔ operation on a constant signal. V_{PD} is simulated by the solid line, V_{Thresh} is simulated by the dashed line, and the comparator output is simulated by the square pulses at the bottom of the plot. V_{Thresh} is modulated using the comparator output bits. This simulation shows that even with zero signal integration a bit stream is still produced, which will need to be subtracted from exposures.

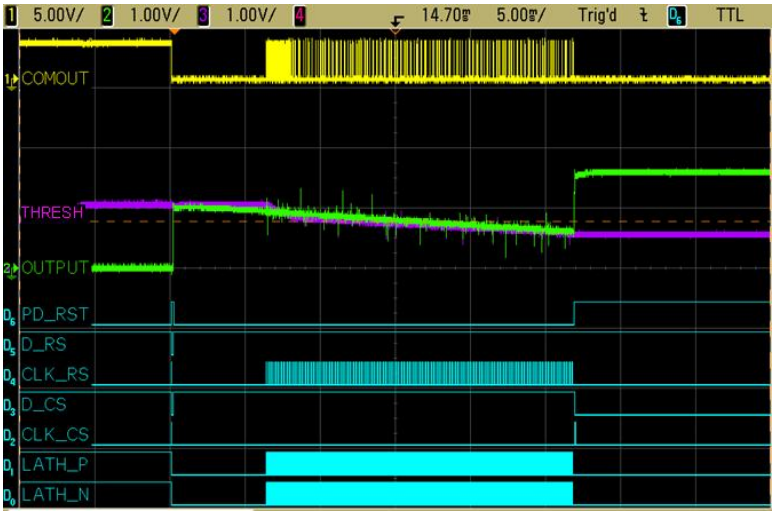

Figure 5. Scope trace of ΣΔ readout of a single pixel. A single pixel is selected by the row and column shift registers and the photodiode is reset to V_{reset}. V_{PD} (labeled OUTPUT) begins integrating charge after being reset. V_{Thresh} (labeled THRESH) is set to a voltage near the reset level of V_{PD}. The comparator output (labeled COMOUT) is all '1's bits at the beginning of the exposure. This reduces V_{Thresh} until it matches V_{PD}. After matching V_{PD} the comparator output bit stream accurately measures V_{PD}. CDS can be done by only storing the bits after V_{Thresh} matches V_{PD}.

Images are formed from the digital bit stream by summing the '1's received for each pixel. The image in Figure 6 was formed by summing the '1's received for each pixel from the ΣΔ readout. This image was taken at room temperature with 256 comparator samples for each pixel. The exposure time per pixel was less than 100 ms to limit dark current integration. Dead pixels can be seen as black pixels.

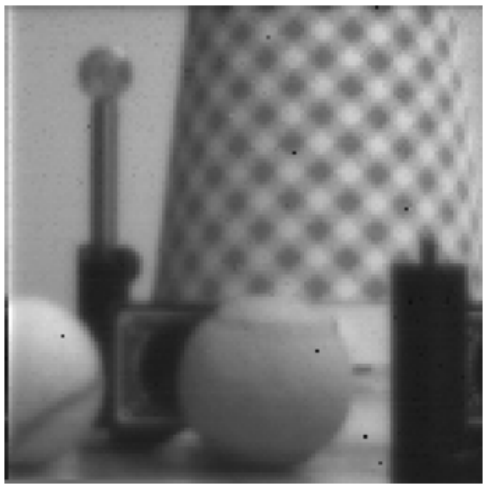

Figure 6. Image from chip formed from the ΣΔ readout. This image was formed by summing the '1's from the ΣΔ readout for every pixel. This image was taken at room temperature with 256 comparator samples for each pixel. The exposure time per pixel was less than 100ms to limit dark current integration. Dead pixels can be seen as black pixels

2.3. Backside Processing

Jet Propulsion Laboratory (JPL) is developing the backside-thinning and delta-doping process for this detector. In the traditional front-illuminated configuration, incident light is subject to absorption and scattering by the multiple layers of oxides, polysilicon, and aluminum that are need to fabricate the CMOS circuit. To back-illuminate a detector, the backside silicon surface is directly exposed to light without any intervening barriers[8]. In addition, for CMOS imagers, the back illumination restores 100% fill factor.

Back-side thinning is performed by utilizing wet etch chemistry to remove the bulk silicon (~200μm thick) substrate down to the epitaxial layer (8μm thick) of the detector[9]. This then allows delta-doping of the epitaxial layer for back-illumination. The thinning process used is a solution of hydrofluoric acid, nitric acid, and acetic acid (HNA) wet etch. The concentration ratio for the acids is selected based on the silicon resistivity. The etch rate of the solution for the bulk silicon is ~2-5μm/min with a total etch time of 124 minutes. While the devices are in the etch bath, they are constantly in motion to prevent large non-uniformities in the etch rate. A second HNA etch with a different concentration ratio is then used (~1 min.) to remove a haze that is typically left on the surface after the bulk silicon is removed. Figure 7 shows a detector after HNA thinning. Non-uniformities are present after thinning and show up as color and intensity variations in the image.

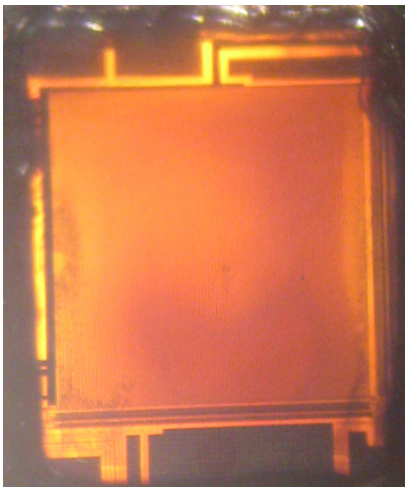

Figure 7. Image taken of a detector die after thinning with HNA wet etch process. The image was taken with a light source behind it to show thinning non-uniformities.

Delta-doping will be done after the thinning process in the next phase of the detector development. Delta-doping provides surface passivation and an electronic potential near the back surface of the detector. The delta-doped layer provides near 100% internal QE in the UV and visible parts of the spectrum. This technique increases the quantum efficiency at short wavelengths because of its effects on the electronic band structure near the surface. The delta-doping process places an extremely high density of dopant atoms ($>10^{14}$ boron atoms/cm^2) within a few atomic layers of the surface with no observable crystal defects and no requirement for post-growth annealing[2,3,4,5]. Because the delta-doped layer is a permanent part of the silicon crystal structure, the resulting improvement in performance is stable and insensitive to environmental conditions.

Results presented in this paper are from pre- and post-thinned detectors. The thinning process is being iteratively studied to optimize detector performance. Die are being processed with different thinning techniques, and laboratory testing is performed to determine detector performance. Fixture design and fabrication as well as growth and temperature calibration for delta-doping this detector are underway.

3. TESTING SETUP

3.1. Testing System

The Rochester Imaging Detector Laboratory (RIDL) has two cryogenic testing systems (see Figure 8) consisting of software and hardware based on a system used to characterize infrared and optical detectors for space- and ground-based applications[10]. The modular architecture of the system allows for rapid acquisition and reduction of large datasets over a broad range of experimental conditions. Minimal effort is required to change between different detectors and different types of detectors. The system can be transported for operation on a telescope.

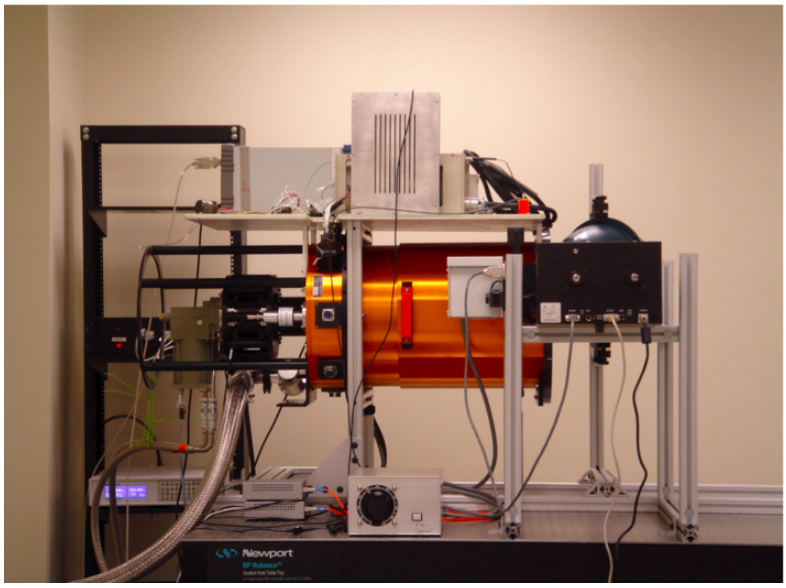

Figure 8. RIDL's cryogenic test system. The vacuum dewar is cooled with a helium cryo-cooler. The detector temperature is controlled using a temperature control module. In the picture is a monochromator and integrating sphere with a calibrated photodiode attached. Post-processing electronics and support electronics are mounted on a plate atop the dewar. Off camera are two data acquisition computers with hardware control software to run the experiment suite.

The system includes a 16 inch diameter dewar (Universal Cryogenics, Tucson, AZ) with a 110 mm diameter CaF_2 window, two cryogenic filter wheels, and a detector enclosure. The system is cooled with a two-stage cooler (CTI Model 1050, Brooks Automation, Chelmsford, MA), and the detector is thermally stabilized with a 10-channel temperature controller (Lakeshore Cryotronics, Westerville, OH). The detector enclosure provides thermal and electrical feedthroughs, an entrance window, and an otherwise light-tight cavity for the detector. The filter wheels can accommodate eight filters and/or radiation sources[11]. Two sets of readout electronics are used: 1) SIDECAR ASIC (SIDECAR) from Teledyne Scientific & Imaging, LLC (Thousand Oaks, CA), and 2) a custom built system based on a DE3 development board from Terasic Technologies (JhuBei City, Taiwan) that uses a Stratix® III FPGA from Altera® (San Jose, CA).

3.2. Data Collection Methods

Two different clocking methods are used for testing: full frame and single pixel. Full frame clocking is analogous traditional raster sampling. After reset, every pixel in the 2D array is sampled once before returning to the first pixel to obtain the second sample. In this mode, the time between two consecutive samples of the same pixel is the time it takes to sample the entire array of pixels once. In single pixel mode, the row and column addressing clocks to a specific pixel. At that point, the row and column addresses are held static and a single pixel is sampled multiple times.

Likewise there are two different readout methods: analog and ΣΔ. In analog readout mode the analog pixel voltage is sent off chip to a set of electronics that amplifies and digitizes the signal. In analog mode, the on chip comparator for the ΣΔ circuit is not operated. In ΣΔ readout mode, described in Section 2.2, the analog output switch is opened which disconnects the V_{PD} from the output pad. This prevents off chip noise injection from feeding into the detector on this line.

The SIDECAR was used to take data with the detector operated in analog readout mode. In this way, the detector is operated like a traditional analog output CMOS detector, which the SIDECAR is designed for. With the SIDECAR, detector properties such as dark current, well depth, linearity, quantum efficiency, etc. can be measured independent of the novel ΣΔ readout.

The SIDECAR is also capable of operating the detectors in ΣΔ readout mode for a single pixel. However, the SIDECAR DAC which is used to supply V_{Thresh} has a high capacitive load because they were designed for low noise static voltage supplies. This limits the sample speed of ΣΔ operation because of the settling time on V_{Thresh}. The SIDECAR system is limited to ~3.5 kHz sample frequency in ΣΔ readout mode. ~3.5 kHz sample frequency is too slow for full frame ΣΔ readout. A full frame exposure with 256 samples of each pixel would take ~30 minutes. A voltage divider was used to achieve a DAC LSB of ~10μV for V_{Thresh}.

A second set of controlling electronics for full frame ΣΔ readout was developed. This system was built using a DE3 development kit from Terasic Technologies based on an Altera® Stratix® III FPGA. DAC daughter cards were used to supply analog voltages including V_{Thresh}. This system has been operated at a sample frequency of up to ~100 kHz. A voltage divider was used to achieve a DAC LSB of 7.8μV for V_{Thresh}. This set of electronics was not configured with a low noise ADC and amplification stage so it was only used for testing in ΣΔ readout mode.

4. CHARACTERIZATION RESULTS

4.1. Converstion Gain/System Gain

In analog readout mode using the SIDECAR there are gains in the signal chain that produce a conversion gain (G_{net}) with units of e^-/ADU as shown in (1).

$$G_{net} = G_{pixel} * G_{UC} * G_{AMP} * G_{A/D} \quad (1)$$

G_{pixel} (e^-/V) is the pixel gain which represents the voltage change per unit charge. It is determined by the photodiode capacitance and is linear over small signal changes. G_{UC} (V/V) is the gain of the pixel source follower FET within each pixel. G_{AMP} (V/V) is the gain of the SIDECAR gain stage which will amplify the signal based on the selectable gain setting. $G_{A/D}$ (V/ADU) is the gain of the ADC within the SIDECAR which converts the analog volts to analog to digital units (ADUs).

When operating in ΣΔ readout mode the SIDECAR specific G_{AMP} and $G_{A/D}$ are no longer relevant, however G_{pixel} and G_{UC} remain part of the net gain (see (2)). An alternative gain is introduced in ΣΔ readout mode, G_{bit} (V/bit). G_{bit} is defined by the voltage change in V_{Thresh} for every bit from the comparator. This is true for both sets of controlling electronics.

$$G_{net} = G_{pixel} * G_{UC} * G_{bit} \quad (2)$$

$G_{A/D}$ was measured in combination with G_{AMP} which gives an equivalent gain that is the product of $G_{A/D}$ and G_{AMP}. The equivalent gain G_{dig} (V/ADU) is measured by dividing the voltage range of a well characterized input sawtooth pattern by the range of ADUs measured. G_{UC} was found by measuring the response to varying reset voltages applied to the gate of the pixel source follower through the reset circuit. G_{pixel} was inferred from (2) and the results of the photon transfer experiment. In this experiment the detector was exposed to a flat field of light from a monochromator and integrating sphere. Non-destructive reads were preformed during an exposure where the signal integration was enough that the noise was photon shot noise dominated. Plotting the variance in each read frame versus the median signal in each read frame will yield a linear relation once the noise is shot noise dominated. The inverse slope of the plot will yield the conversion gain G_{net} (e^-/ADU) (see Figure 9). Table 1 summarizes the gain measurements for a thinned and un-thinned detector. A photodiode capacitance of 36.9 fF was calculated for the un-thinned detector. The thinning process changed the photodiode capacitance to 28.6 fF. The calculated photodiode capacitance matches the expected value (~30 fF). G_{bit} varies by experiment and was calculated based on the measured DAC LSB and the specific V_{Thresh} modulation setting for a given experiment. It was assumed that the G_{pixel} and G_{UC} are the same for APS and ΣΔ readout because the photon transfer curves gave similar results.

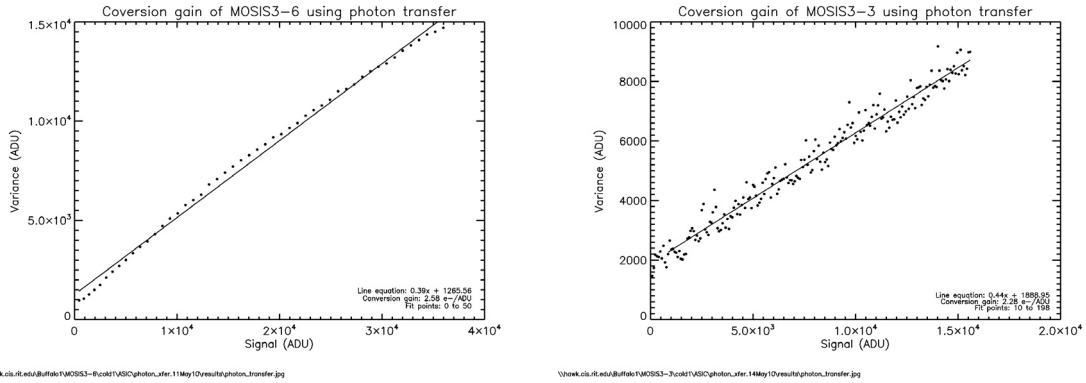

Figure 9. Photon Transfer plots for an un-thinned (*left*) and thinned (*right*) detector. G_{net} changed from 2.56 e^-/ADU to 2.28 e^-/ADU after thinning.

Table 1. Table of gains

Detector	G_{net} (e^-/ADU)	G_{Dig} (μV/ADU)	Unit Cell Gain (μV/ADU)	G_{UC} (V/V)	$1/G_{pixel}$ (μV/e^-)	Photodiode Capacitance (fF)
Un-thinned (MOSIS3-6)	2.58	8.07	11.18	0.72	4.33	36.93
Thinned (MOSIS3-3)	2.28	8.07	12.57	0.64	5.59	28.63

4.2. Well Depth and Linearity

The well depth and linearity give measurements for the total number of electrons that can be accumulated in a photodiode and the photodiode response to charge integration. The well depth and linearity was measured in analog full frame readout with the SIDECAR. The detector was illuminated with a flat field from a monochromator and integrating sphere. Non-destructive up-the-ramp reads were done through saturation of the detector. The *top left* plot in Figure 10 shows the full well was 294 ke$^-$ with a variation of ~4% for the un-thinned detector. When compared to the same measurement made on the thinned device (*top right* in Figure 10), the full well did not significantly change. The region used for reduction was different for the thinned and un-thinned detectors because non-uniformity in the thinning process could skew the results. This non-uniformity should be removed from future iterations of the thinning process. The *bottom* plots in Figure 10 show the normalized slopes of each sequential read pair with respect to the slope of the 0^{th} to 1^{st} read. The detectors had a linear response within ~5% over 90% full well for both thinned and un-thinned. The non-linearity is well characterized by a second order polynomial which suggests it could be corrected for and removed.

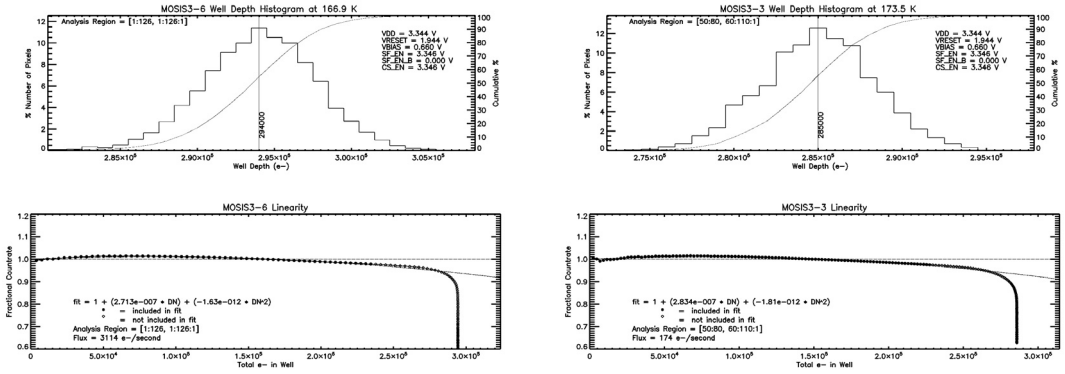

Figure 10. Well depth plots for an un-thinned (*top left*) and thinned (*top right*) detector show a full well of 294 ke^- which was not significantly changed by the thinning process. The linearity plots for an un-thinned (*bottom left*) and thinned (*bottom right*) detector show a linear response of ~5% over 90% full well.

4.3. Dark Current

Dark current is a measure of thermally generated electrons and is dependant on temperature. The dark current was measured in two different ways. The first measurements were done by measuring the mode of the signal in each frame of a series of non-destructive up-the-ramp reads while the detector was isolated from any external photon source. The slope of the mode through the up-the-ramp reads was calculated and reported as the dark current. This was repeated for different temperatures to determine the temperature dependence. Figure 11 shows the dark current versus temperature for both a thinned and un-thinned detector. The thinning process increased the dark current by about a factor of 2 at ~166K. Figure 12 shows the histogram of dark current for both an un-thinned and thinned detector at ~166 K. This histogram is made by calculating the per pixel slope of signal integration in an up-the-ramp exposure. The histograms show a significant number of pixels that had high dark current. Figure 13 shows an image of the per pixel dark current at ~166K for an un-thinned (*left*) and thinned (*right*) detector. The pixel values in this image are the per pixel slopes calculated from the signal integration in each pixel. The images show the increase in dark current after thinning is a uniform increase in the per pixel dark current. In other words, the thinning process did not cause a specific region of increased dark current; rather it was a uniform increase in the dark current of all pixels.

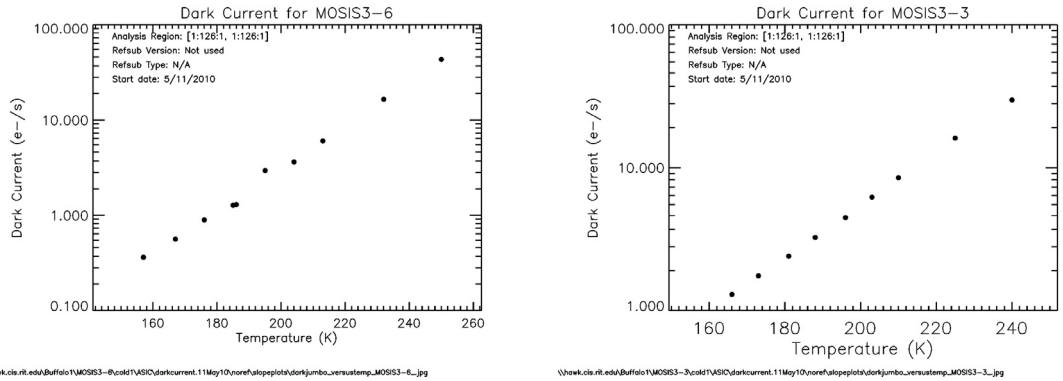

Figure 11. Dark current versus temperature for an un-thinned (*left*) and thinned (*right*) detector. Points on these plots were made by measuring the mode of the signal in each frame of a series of non-destructive up-the-ramp reads while the detector was isolated from any external photon source. The slope of the mode through the up-the-ramp reads was calculated and reported as the dark current. This was repeated for different temperatures to determine the temperature dependence. The dark current was increased by a factor of ~2 after thinning.

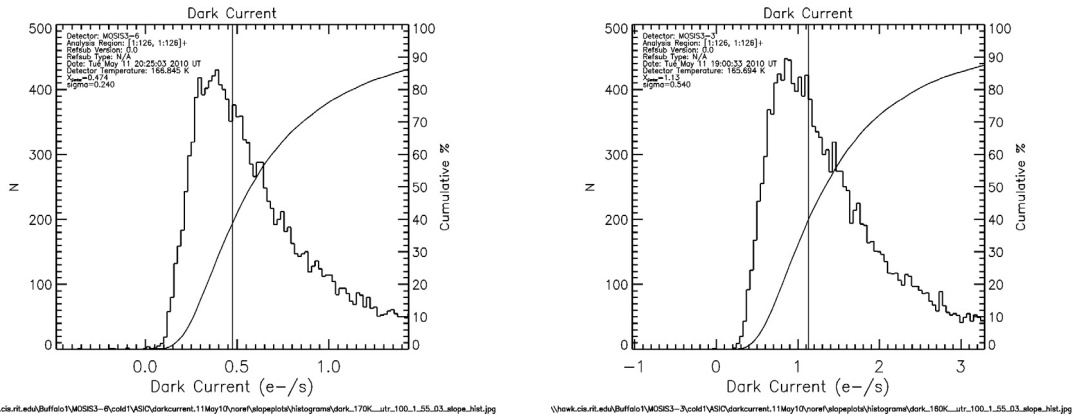

Figure 12. Dark current histograms for an un-thinned (*left*) and thinned (*right*) detector at ~166K. These histograms were made by calculating the per pixel slope of signal integration in an up-the-ramp exposure. The histograms show a significant amount of pixels that had high dark current.

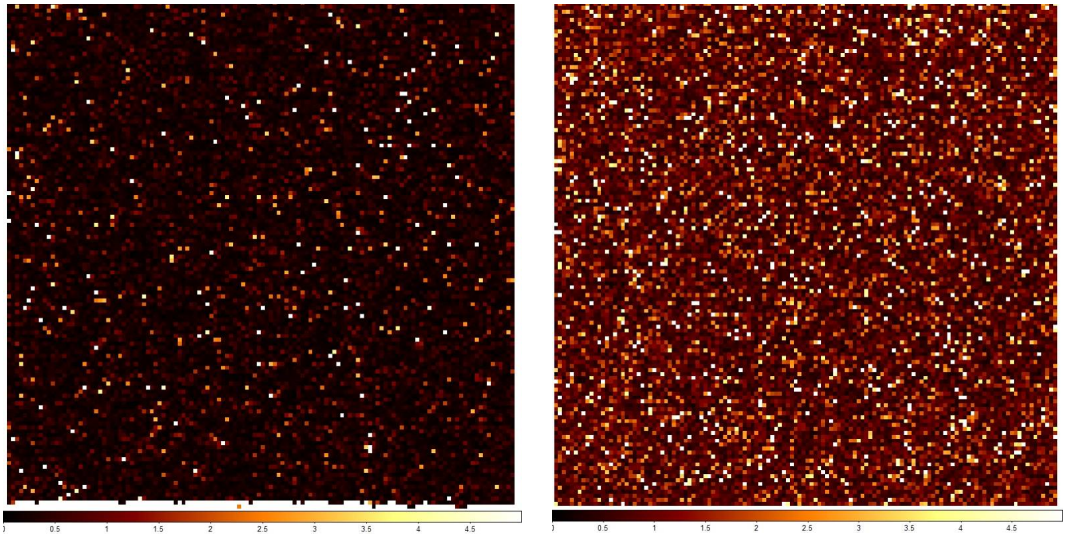

Figure 13. Image of the per pixel dark current at ~166K for an un-thinned (*left*) and thinned (*right*) detector. The pixel values in this image are the per pixel slopes calculated from the signal integration in each pixel. The images show the increase in dark current after thinning is a uniform increase in the per pixel dark current. In other words, the thinning process did not cause a specific region of increased dark current, rather it was a uniform increase in the dark current of all pixels. Note the scale for these images is ADU.

4.4. Relative Quantum Efficiency (RQE)

Detective Quantum Efficiency (DQE) is the ratio of the square of the measured signal to noise to that of an ideal detector. Most measurements are made with significantly high fluence so that read noise does not affect the measurement. The first part of measuring DQE is to measure the relative quantum efficiency RQE. RQE was measured by illuminating the detector with monochromatic flat field illumination produced by a monochomator and integrating sphere. A calibrated photodiode mounted on the integrating sphere was used to measure the flux. The detector was then read out in two non-destructive reads to create a CDS image. This was repeated for wavelengths from 300 nm to 1200 nm in 5 nm steps. The detector response was then compared to the calibrated photodiode response to give RQE. Future measures are needed to turn the RQE results presented here into DQE results. To measure DQE, a second calibrated photodiode needs to be placed at the location of the detector to map the flux at the integrating sphere to the flux at the detector. RQE results can be useful in measuring the shape of the spectral response. RQE is also useful for determining how process steps change the spectral response. Figure 14 displays the RQE results for both an un-thinned (*left*) and thinned (*right*) detector. The QE axis is normalized to the highest response measured in each experiment. Both detectors were frontside illuminated. The plots show the thinned chip has a lower response at longer wavelengths as compared to the un-thinned chip.

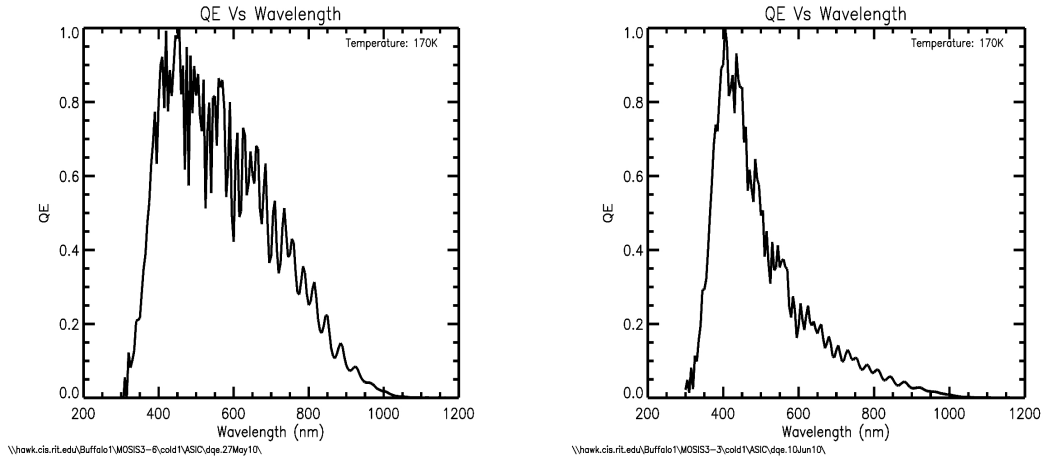

Figure 14. RQE results for both an un-thinned (*left*) and thinned (*right*) detector. The QE axis is normalized to the highest response measured in each experiment. Both the detectors were frontside illuminated. The plots show the thinned chip has a lower response at longer wavelengths as compared to the un-thinned chip.

The Monochromatic flat field on the thinned detector gave an opportunity to measure the uniformity of the detector surface. Figure 15 (*right*) shows an image taken of the thinned chip with a light source directly behind it. Thickness variations present as color and intensity changes. Figure 15 (*left*) shows an image taken by the detector while 600 nm monochromatic light is shown on it. The pattern of repeating light and dark are fringing patterns caused by interference between incident and reflected light off the back of the thinned detector. The fringing patterns match the image of the detector showing a thickness variation. A significant thickness change can be seen at the bottom of both the images. By counting the number of fringes, the thickness variation is estimated to be ~3 µm from maximum peak to minimum valley.

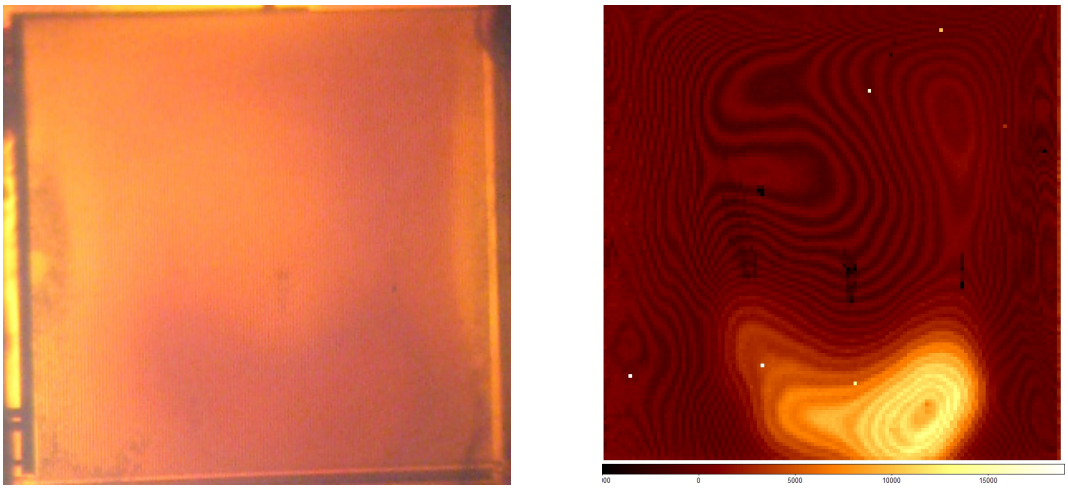

Figure 15. (*right*) Image of the thinned chip with a light source directly behind it. Thickness variations present as color and intensity changes. (*left*) Image taken with the detector while 600 nm monochromatic light is shown on it. Fringing pattern can be seen that match with the image taken of the detector (*right*). A maximum thickness variation across the array was estimated to be ~3 µm.

4.5. Read Noise

Read noise is a measure of the uncertainty in measuring the photodiode signal. Initial noise measurements were made by sampling a single pixel with the ΣΔ readout. To do this a single pixel was reset, exposed, and sampled 1024 times with the ΣΔ readout. This was repeated to get many exposures of the same pixel. For each exposure the first 256 samples were ignored as they were used to do CDS subtraction. The number of '1's in the bit stream were summed for different number of comparator samples. The standard deviation of the sum was then computed for each set of total comparator samples. The comparator sample frequency for this experiment was ~3.5 kHz with an exposure time of ~300 ms. The threshold was modulated up 10 μV when the comparator output was '0' and down 20 μV when the comparator output was '1'. The plot in Figure 16 shows the read noise (μV) versus the total number of comparator samples summed. The read noise was calculated for total comparator samples of 2, 4, 8, 16, …, 768. A read noise of 16.2 – 18.9 μV was measured on an un-thinned detector. The noise translates to 3.8 – 4.4 e^-, given the conversion gain for this detector was 4.3 μV/e^-.

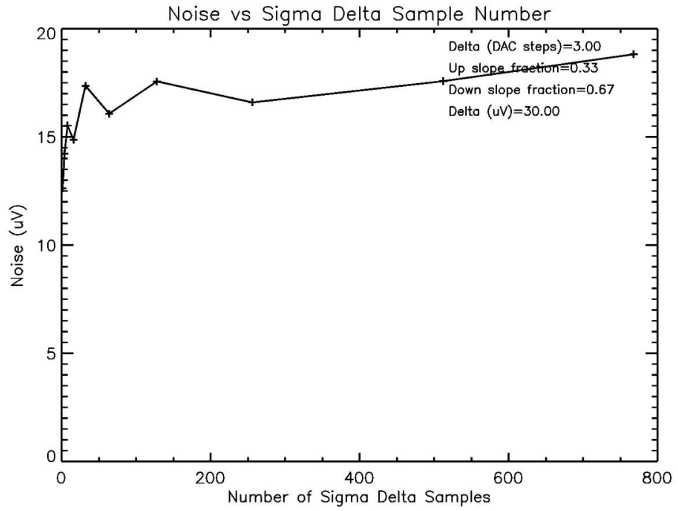

Figure 16. Plot shows read noise (μV) versus the total number of comparator samples summed for ΣΔ readout of a single pixel. The read noise was calculated for total comparator samples of 2, 4, 8, 16, …, 768. The comparator samples were taken at a frequency of ~3.5 kHz. A read noise of 16.2 – 18.9 μV was measured on an un-thinned detector. The noise translates to 3.8 – 4.4 e^-, given the conversion gain for this detector was 4.3 μV/e^-.

5. CHIP RE-DESIGN AND RESULTS

5.1. Photodiode

A re-designed chip was fabricated to improve upon the chip tested for this paper. The re-designed chip has a reduced photodiode capacitance which will increase the $1/G_{pixel}$ (μV/e^-) conversion. The new design reduced the photodiode capacitance by a factor of 5. By reducing the capacitance, the voltage induced by a photo-generated electron will increase. The read noise of the ROIC is expected to be independent of the photodiode capacitance. This means that while the read noise in units of μV will remain the same, the read noise in units of e^- will be reduced. The photodiode capacitance, G_{bit}, G_{pixel}, and G_{net} for the re-designed detector are shown in Table 2. A 7.6 fF photodiode capacitance was calculated. The inverse pixel gain ($1/G_{pixel}$) was inferred using G_{bit} and G_{net} measured from the photon transfer experiment to be 21.2 μV/e^-. The photon transfer experiment was run using the FPGA readout electronics in ΣΔ readout

of a single pixel. The photodiode capacitance was reduced by a factor of 5.1 which agrees with the expected reduction. Reducing the capacitance will reduce the full well capacity of the detector; the full well is expected to reduce to ~60ke$^-$.

Table 2. Table of gains for the re-designed detector

Detector	G_{net}	G_{bit}	$1/G_{pixel}$	Photodiode Capacitance
	(e^-/bit)	(μV/bit)	(μV/e^-)	(fF)
Un-thinned (MOSIS4-1)	7.39	156.3	21.15	7.56

5.2. On Chip DAC

The re-designed detector also has an on-chip DAC to supply V_{Thresh}. Having an on-chip DAC eliminates potential noise pickup on the analog V_{Thresh} being supplied off chip. Also, the re-designed detector will be able to run faster because the on-chip DAC will reduce the capacitive load on V_{Thresh}. Less capacitive load means the settling time on the analog voltage modulation reduces which was a limiting characteristic in the previous design. The design for the on-chip DAC is an 8 bit DAC with the voltage range set by a V_{high} and V_{low}. The resolution of the on chip DAC will be V_{LSB} as defined in (3). This design still allows for adjustment of the threshold modulation steps which allow for operation in low and high flux environments. The re-design detector is currently being characterized including the capabilities of the on-chip DAC.

$$V_{LSB} = (V_{high} - V_{low})/256 \tag{3}$$

5.3. Read Noise

An initial read noise measurement was made in ΣΔ readout of a single pixel. Similar to the read noise measurement on the previous design the pixel was reset, exposed, and sampled 2048 times with the ΣΔ readout. This was repeated to get many exposures of the same pixel. For each exposure the first 800 samples were ignored as they were used to do CDS subtraction. The number of '1's in the bit stream were summed for different number of comparator samples. The standard deviation of the sum was then computed for each set of total comparator samples. The comparator sample frequency for this experiment was ~3 kHz with an exposure time of ~600 ms. The threshold was modulated up 7.8 μV when the comparator output was '0' and down 7.8 μV when the comparator output was '1'. The plot in Figure 17 shows the read noise (μV) versus the total number of comparator samples summed. The read noise was measured to be 45.8 – 90.1 μV. Using the inferred inverse pixel gain ($1/G_{pixel}$) for this detector (21.2 μV/e^-) the equivalent noise was 2.2 – 4.3 e^-.

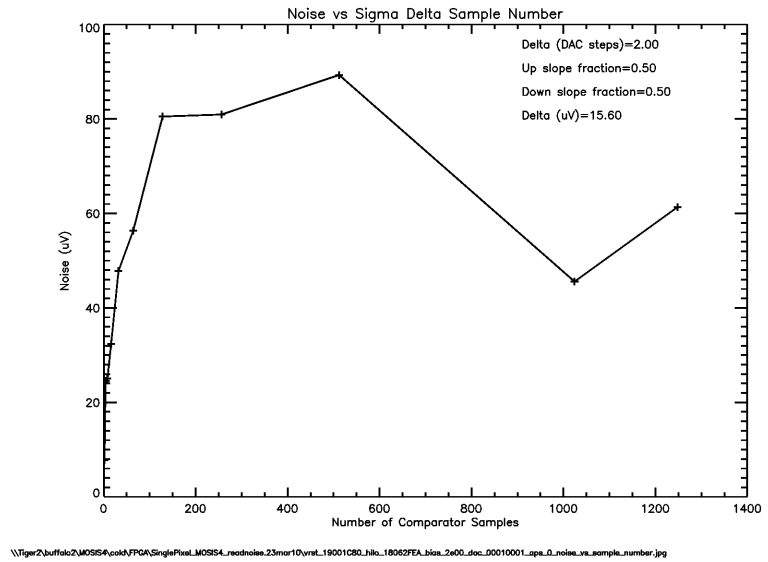

Figure 17. Plot of ΣΔ read noise (μV) versus the total number of comparator samples summed. Exposures were taken of a single pixel on an un-thinned detector at ~170K with a comparator sample frequency of ~3 kHz. The read noise was measured to be 45.8 – 90.1 μV. Using the $1/G_{pixel}$ for this detector (21.2 μV/e^-) the equivalent noise was 2.2 – 4.3 e^-.

6. DISCUSSION

The ΣΔ-based monolithic CMOS detector design is promising based on the current test results. The single pixel read noise is 3.8 – 4.4 e^- for the first design and 2.1 – 4.2 e^- for the re-designed detector. With further hardware optimization, input bias noise reduction, clock timing changes, the noise is expected to be less. Supplying V_{Thresh} with an external DAC limits the sampling frequency of the ΣΔ readout. Read noise results presented in this paper were taken with a sample frequency of ~3.5 kHz. The re-designed detector addresses this problem with an on-chip DAC for V_{Thresh}. The re-designed detector will be able to operate at faster sampling frequencies, although it remains to be fully tested. Additionally, full frame ΣΔ read noise is being measured and compared to the single pixel read noise.

The thinning process did not significantly change the detector characteristics measured, with the exception of the dark current and the relative quantum efficiency. The dark current of the un-thinned detector was high at ~0.6 e^-/second/pixel at ~166K and was further increased by the thinning process to ~1.0 e^-/second/pixel. The thinning process was expected to increase the dark current however the un-thinned dark current was already higher than desired. Leakage current in the ROIC is being investigated as a source of signal integration during dark exposures. The leakage current would present as dark current in our experiment. Additionally, delta-doping is expected to reduce the post-thinning dark current increase[2,3,4,5]. The relative quantum efficiency for the pre- and post-thinned detectors were as expected with a peak near 400-450 nm and a low response at the longer wavelength. The reduced red response after thinning was expected due to substrate removal. Delta-doping is expected to increase the spectral response especially in the short wavelengths[2,3,4,5]. A system calibration will be done to convert the relative quantum efficiency results to detective quantum efficiency.

Experiments are continuing to determine the optimal thinning process. A combination dry/wet etch process is being tested. This combines a plasma and HNA process to etch the bulk silicon substrate. Current results suggest it may be a more uniform process and reduce the thickness variations after thinning.

Further comparison studies need to be done to validate that the re-designed detector's performance surpasses the previous design's performance. However, the project is expected to move away from the previous design and continue

with the re-design detector. The re-design detector will be characterized pre- and post-thinning similar to results presented here and then characterized pre- and post-delta-doping.

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