Large Format Short-wave HgCdTe Detectors and Focal Plane Arrays

Richard E. Bornfreund, Peter J. Love, Alan W. Hoffman, Ken J. Ando, Elizabeth Corrales, William D. Ritchie, Neil J. Therrien, Joe P. Rosbeck, Aimee Buell, Jeffrey Peterson, Jeffrey Franklin, Mauro Vilela, J. Bangs, Scott M. Johnson, and William Radford.

Raytheon Vision Systems, 75 Coromar Drive, Goleta, CA 93117

ABSTRACT

Raytheon Vision Systems has been actively pursuing the development of large format HgCdTe short-wave focal planes. The predominant interest in SWIR focal planes is being driven by the astronomy community which requires extremely low dark current due to the low backgrounds involved with stellar observation.

A major effort for SWIR focal planes at RVS is the United Kingdom's Visible and Infrared Survey Telescope for Astronomy (VISTA) program, for which RVS is currently delivering 16 2048 x 2048, 20 μm focal plane arrays. Details on the project together with the performance being achieved on the focal plane arrays will presented.

The readout integrated circuit (ROIC) used for this focal plane is the VIRGO SB301 ROIC which is 3-side buttable allowing for mosaic focal plane arrays as large as 4Kx2nK format. The ROIC utilizes a PMOS based source follower per detector input circuit with a charge capacity of $2x10^5$ electrons and has a read noise of 18 e- rms with off-chip Double Correlated Sampling.

The detector material baseline for the VISTA product is liquid phase epitaxially (LPE) grown HgCdTe on Cadmium Zinc Telluride (CZT) substrates. A number of science grade 2048 x 2048, 20 μm focal planes have been produced with response operabilities of > 99.5 %, anti-reflection coated (ARC) quantum efficiencies > 80 % and dark currents < 1 e-/s. Response operability has been defined as between 0.7 and 1.4 times the mean array response.

With the advent of larger telescopes, larger size SWIR focal plane arrays are envisioned. To evaluate the benefits using SWIR grown by molecular beam epitaxy (MBE) on larger silicon wafers, which allow larger detector arrays to be fabricated than available from CZT substrates, RVS has processed and assembled an MBE SWIR HgCdTe detector to the VISTA architecture. The results will be presented. Excellent performance has been achieved, with a response operability of 99.4 %, a non-antireflection coated (ARC) K-band quantum efficiency (QE) of the MBE array was 55 % (projected to be 73 % with an ARC) and a mean dark current of 0.47 e-/s. The performance was very comparable to the VISTA LPE HgCdTe on CdZnTe focal planes.

Keywords: VIRGO, VISTA, NIR, FPA, SCA, SWIR HgCdTe, MBE, HgCdTe on Si, SFD, Large-format, mosaic

1. INTRODUCTION

The demand for large-format near infrared (NIR) arrays has grown for both ground-based and space-based applications. These arrays are required for maintaining high resolution over very large fields of view for survey work. Raytheon Vision Systems (RVS) is meeting this market through the development of new fabrication techniques for large ROICs, enhancement of the LPE HgCdTe/CdZnTe production process to maximize substrate utilization, and the development of HgCdTe grown by molecular beam epitaxy on commercially available 4" and 6" silicon substrates.

For the Astronomy market, RVS has produced a new Readout Integrated Circuit (ROIC) that can be fabricated in integer m × n multiples of a basic 512 × 1024 format building block using Reticle Image Composition Lithography (RICL). The ROIC, referred as the VIRGO array,[1] and the module package which houses the 2K × 2K Sensor Chip

Assembly (SCA) have been designed to be 3-side buttable for fabrication of large mosaic arrays of 4K × 2nK format. The first major application of this array will be for the United Kingdom's Visible and Infrared Survey Telescope for Astronomy (VISTA),[2,3,4] which will require 16 science-grade 2K × 2K modules. VISTA is designed to operate in the z´, J, H, and K_s bands between about 1 micron and 2.5 microns. The Shortwave Infrared (SWIR) HgCdTe detectors will operate near 80 K. Key requirements for the VISTA detectors are shown in Table 1.

The following sections will briefly describe the SWIR Photovoltaic (PV) HgCdTe detectors, the VIRGO ROIC, and the 2K × 2K module package. Additional details on the detectors, VIRGO ROIC, and module package may be found in a previous publication.[5] Summary data will be shown for several recently delivered VISTA modules together with detailed data on a particular module, module 24 and finally module performance results for MBE grown HgCdTe on Si detectors hybridized to the Virgo ROIC will be presented.

Table 1. Key VISTA detector performance requirements.

Parameter	Requirement	Measured
Format and pitch	2K × 2K with 15.5 μm ≤ pitch ≤ 20.5 μm	2048 × 2048 with 20 μm pixel pitch
Operating temperature	77 K ± 5 K	78 K
Well capacity	> 1.0×10^5 electrons	> 2.0×10^5 electrons
Wavelength range	1.0 to 2.5 μm (goal: 0.85 to 2.5 μm)	0.85 to 2.5 μm
QE J band (1.13 to 1.35 μm): H band (1.50 to 1.80 μm): K_s band (2.02 to 2.30 μm):	 QE > 38% QE > 47% QE > 47%	> ~70% in all spectral bands with a single-layer AR coating (minimum reflectance at 1.4 μm)
Uniformity of QE	< 10% (sigma/mean) in all wavebands	< 10% (sigma/mean) in all wavebands
Read noise	≤ 32 e- rms with off-chip CDS (at ≥ 1.0 Hz frame rate)	≤ 20 e- rms with off-chip CDS (at ≥ 1.0 Hz frame rate)
Dark current	< 8 e-/sec/pixel at 77 K	< 4 e-/sec/pixel at 78 K
Non-linearity	< 3% up to 80% of full well	< ± 0.3%
Fill factor	> 90%	> 98%
Defects (operability)	Operability > 96% (dark current and QE)	> 98%
Detector physical flatness	< 12 μm	< 6 μm

2. SWIR PV HgCdTe/CdZnTe DETECTORS

The SWIR PV p-on-n HgCdTe detectors are grown by Liquid Phase Epitaxy (LPE) on bulk, lattice-matched CdZnTe substrates. At the current size limit of readily available CdZnTe substrates, less than roughly 6 cm × 6 cm, only a single 2K × 2K detector with 20 micron pitch can be fabricated on a substrate. The detector cutoff wavelength can be adjusted over a range from as short as ~1.5 microns to 2.5 microns or longer, as needed. Completed detectors are hybridized to the Si ROIC through indium bump interconnects. Due to the large thermal expansion coefficient mismatch between the HgCdTe detector and the Si ROIC, a shim structure is bonded to the ROIC to force the ROIC to contract at the same rate as the HgCdTe during cooldown. The HgCdTe detector is backside-illuminated through the bulk CdZnTe substrate, which is opaque to radiation with wavelengths shorter than about 0.85 microns. To extend response from the NIR into the visible region, the CdZnTe detector substrate can be removed. With no anti-radiation (AR) coating, the reflection loss at the vacuum/CdZnTe substrate interface is about 21%. Since the internal Quantum Efficiency (QE) for the detector approaches 100%, a suitable AR coating can provide total external quantum efficiencies of greater than 90% over a fairly broad spectral range.

3. VIRGO SB301 READOUT INTEGRATED CIRCUIT

The VIRGO SB301 CMOS Si ROIC was developed to meet a variety of needs for large-format arrays which operate under low-background conditions[1]. The unit cell input circuit is a 3-transistor Source Follower per Detector (SFD). The chip can be fabricated in integer multiples of a 512 (horizontal) × 1024 (vertical) format, allowing multiple formats to be fabricated with the same mask set. This is accomplished using a type of reticle "stitching" dubbed Reticle Image Composition Lithography (RICL). For VISTA, nine 2K × 2K arrays and eight 1K × 1K arrays are printed on an 8-inch wafer. Although the ROICs fabricated to date have been only up to 2K × 2K in size, a 4K × 4K VIRGO ROIC could easily be fabricated on an 8-inch wafer.

The VIRGO SFD input circuit (see Figure 1) achieves a well capacity of $>2 \times 10^5$ electrons and a read noise of less than 20 e- rms with off-chip Correlated Double Sampling (CDS). Other features of the VIRGO array include 4 or 16 outputs (programmable), and a frame rate of up to 1.5 Hz in 16-output mode. The chip is designed to run at about a 280 kHz data rate (1 Hz frame rate with 16 outputs). Power dissipation is about 7 mW at a 1 Hz frame rate in 16-output mode. Reset modes include both global reset and reset by row (ripple mode). Figure 2 illustrates the basic floor plan of the VIRGO ROIC. Reference pixels are built-in to the output data stream: row 0 is a reference row with the pixels held at the starvation level (reset level) and row 2049 is a reference row with the pixels held at the saturation level. Thus, to read out the entire array, a total of 2050 rows must be read out. In addition, in 16-output mode, each row consists of 134 pixel periods on each output: 128 active pixels plus 6 reference pixels at the starvation level. A total of 36 unique I/O pads are brought out to operate the chip, including 16 analog outputs, 2 clocks (master clock and frame start clock), 2 current sources, 3 control lines, and 13 bias lines.

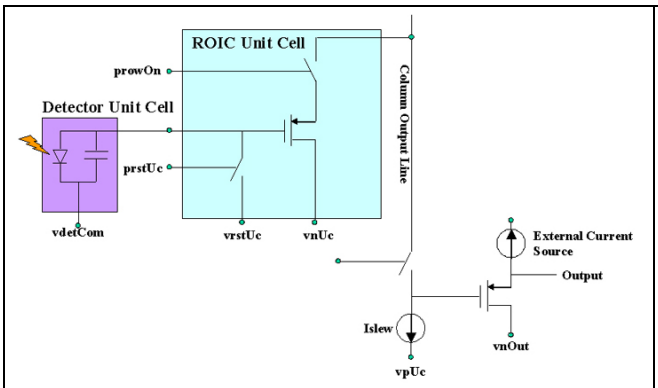

Fig. 1. VIRGO SB301 ROIC unit cell consists of a 3-transistor SFD. The output stage consists of another source follower circuit which requires an external current source.

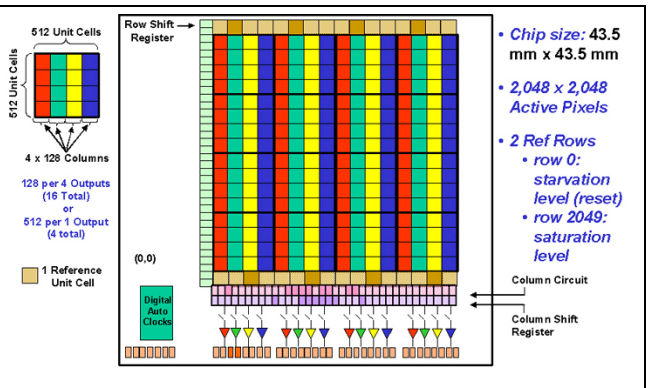

Fig. 2. Floor plan of the VIRGO SB301 2K × 2K ROIC. The 2048 × 2048 active pixels are read out in blocks of 128 or 512 columns each through either 4 or 16 outputs (selectable).

4. 2K × 2K MODULE PACKAGE

The 2K × 2K module package for VISTA is a reliable, robust 3-side buttable package which allows the fabrication of large mosaic arrays of 4K × 2nK format (see Figure 3). Since each module is designed to be identical, all modules are interchangeable. Figure 4 shows some of the details of the module architecture. The module consists of an SCA mounted to a metal pedestal to which a thermal flex cable is mounted. A multilayer ceramic motherboard provides the electrical connections between the SCA and the cable, and also supports surface-mount components including heaters, temperature sensors, resistors, and capacitors. The module is designed to be easily integrated onto a platform with "plug-and-play" operation. This is accomplished with three simple interfaces: a mechanical interface which allows automatic alignment in x, y, and z through precision datums on the module pedestal; an electrical interface through a thermal flex cable with a 51-pin MDM connector; and a thermal interface which consists of a cold strap attachment to the back of the module pedestal. For VISTA, 16 modules are mounted in a 4 × 4 configuration on a "plate" to form the mosaic focal plane array. VISTA does not require butting of adjacent modules. However, for applications which require butting of modules on all four sides, a "3½-side" buttable module package has also been designed. The fourth side of this module provides room only for wire bonds between the ROIC and the top surface of the multilayer motherboard. All surface-mount components are mounted on the underneath side of the motherboard and the cable lies in a plane perpendicular to the focal plane and motherboard surfaces.

5. DARK CURRENT

Low-level dark current measurements are difficult because the measurement can easily be contaminated with dewar light leaks or read glow from the MUX. For these reasons, dark current measurements at or below the 1 e-/sec level often represent only an upper limit on the true detector dark current.. The "standard" method we employed for measuring dark current on VISTA modules was to acquire 10 frames while "sampling-up-the-ramp" after a single reset. During readout, the array was always read out at 1 sec per frame, but in between reads a "dead" time of two minutes was inserted in which the master clock was turned off and no rows were enabled. Dark current was then estimated by either a) performing a linear regression fit to the 10 samples and deriving the dark current from the best-fit slope, or b) taking the difference between two frames, say frame 10 and frame 4, and dividing by the time interval between the two frames. This method is convenient since it requires a total acquisition time of only 20 minutes, however, longer integration times are needed to measure dark currents of order ~0.1 e-/sec or less.

Figure 5 shows an example of a measurement of array-average Dark Signal versus time at 78 K by sampling up the ramp with a 6-minute (360 sec) dead time between reads. The dark current derived from the best-fit slope is 0.24 e-/sec (Zt = 3.0 µV/e- and gain = 10 for dark signal acquisition).

Fig. 3. VISTA 2K × 2K 3-side buttable module package. A single SCA is mounted on a metal pedestal which supports a thermal flex cable with a 51-pin MDM connector.

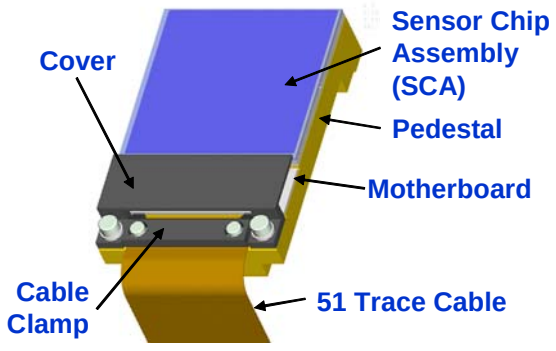

Fig. 4. Details of the VISTA 2K × 2K module package showing the SCA, motherboard, pedestal, cable, cable clamp, and cover.

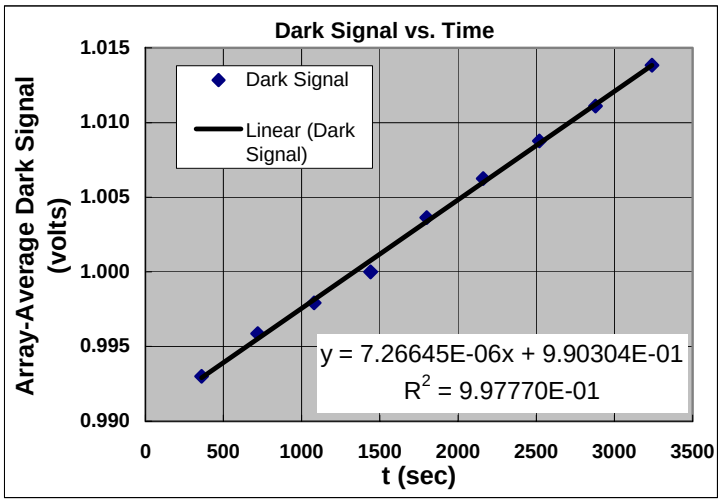

Fig. 5. Array-average Dark Signal versus time measured by sampling up the ramp with 6-minute dead periods between reads. From the best-fit slope, the mean dark current is 0.24 e-/sec at 78 K.

6. PERFORMANCE SUMMARY FOR SEVERAL VISTA MODULES

A summary of the performance of several VISTA modules is shown in Figure 6. Array-average quantum efficiency is shown in Figure 6a for the J, H, and K bands. These values reflect the average of all 2048 × 2048 active pixels on each array. In Figure 6b, the QE uniformity is shown for the same modules (sigma/mean in %). All modules meet the VISTA QE requirements in all three spectral bands (J-band: > 38%; H- and K-bands: > 47%). In addition, all modules meet the QE uniformity requirement of < 10% sigma/mean with the exception of the J band on two modules (see Figure 6b).

Similar results are shown for Dark Current in Figure 7 for the same modules for which QE data is shown in Figure 6. Dark Current was measured at 78 K.

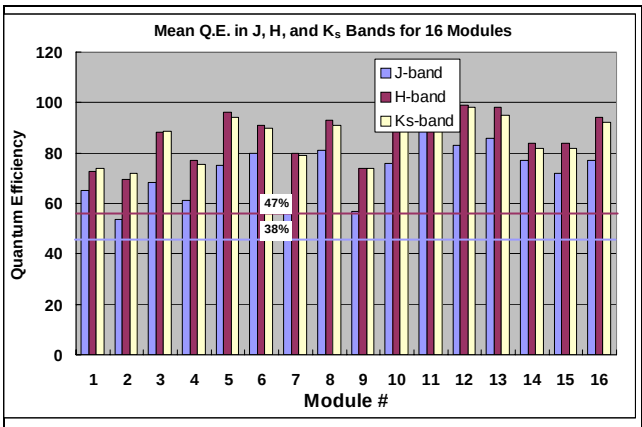

Fig. 6a. Mean QE in the J, H, and K bands for the 16 VISTA flight modules. The VISTA QE requirement is QE J > 38% and QE H, Ks > 47%.

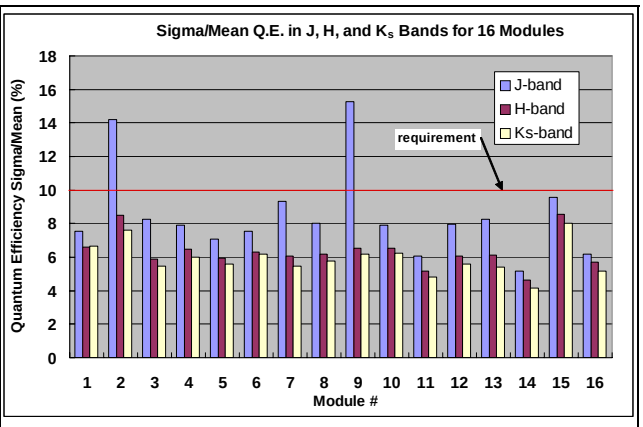

Fig. 6b. Uniformity of QE in the J, H, and K bands for the 16 VISTA flight modules. The VISTA requirement is QE sigma/mean < 10%.

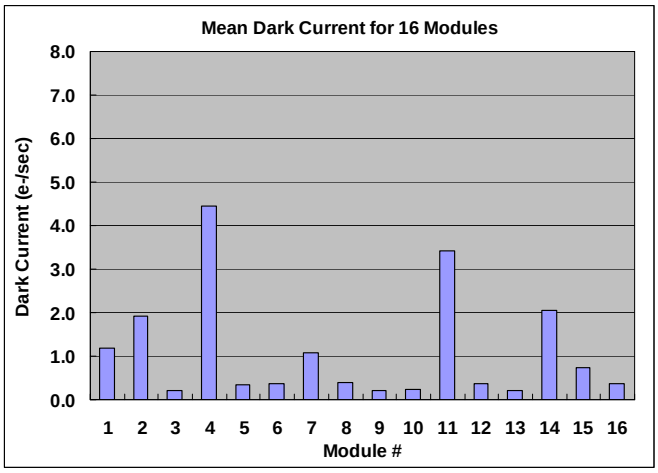

Fig. 7. Mean Dark Current at 78 K for the 16 VISTA flight modules. The QE data is shown in Figure 5.

7. SCA/MODULE DATA FOR SCIENCE GRADE MODULE 41

To date, several "bare-MUX" modules, two Engineering modules, and all sixteen Science Grade modules have been delivered to the United Kingdom Astronomy Technology Centre (UK ATC). Sample data for one of the Science Grade modules, module 41, is shown in this section. Data for another module, 22, is reported in another paper.[6] As described above, this module received a single-layer AR coating with a minimum in reflectance at a wavelength of about 1.4 microns. Figure 8a shows a map of QE in the J band for the entire 2048 × 2048 active array. Figure 8b shows the associated QE histogram. The mean QE in the J band is 83.0% with a uniformity (sigma/mean) of 7.98%. QE operability for the entire 2048 × 2048 array in the J band is 99.59%.

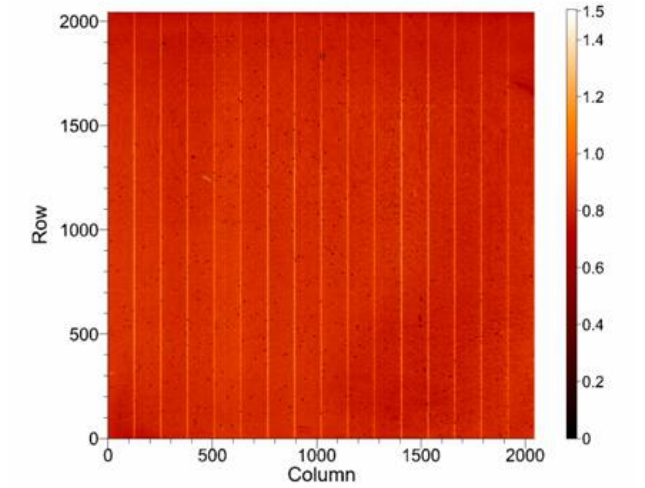

Fig. 8a. Module 41 QE in the J band. The mean QE is 0.830 and the standard deviation is 0.070 (7.98 % sigma/mean). QE operability is 99.59%.

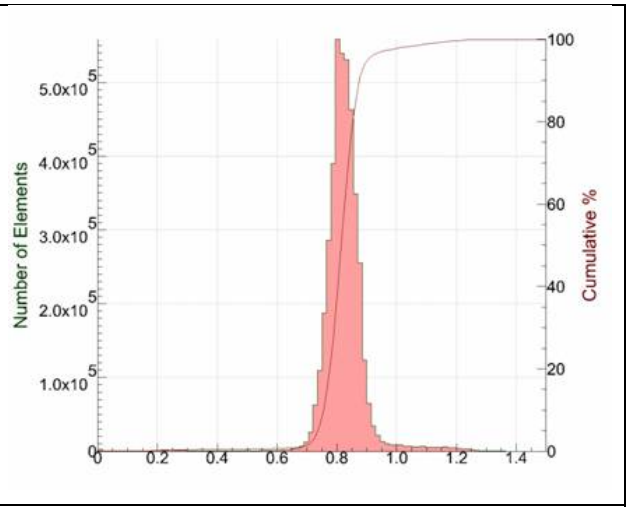

Fig. 8b. Module 41 QE histogram in the J band.

Figures 9 and 10 show similar data for the H and K bands. For the H band, the mean QE is 99.0% with a uniformity (sigma/mean) of 6.06%. QE operability for the entire 2048 × 2048 array in the H band is 99.62%. For the K band, the mean QE is 98.0 % with a uniformity (sigma/mean) of 5.6%. QE operability for the entire 2048 × 2048 array in the H band is 99.73%.

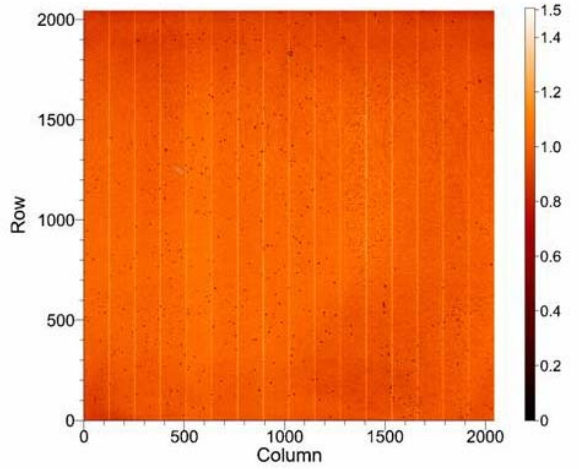

Fig. 9a. Module 41 QE in the H band. The mean QE is 0.913 and the standard deviation is 0.099 (6.1% sigma/mean). QE operability is 99.62%.

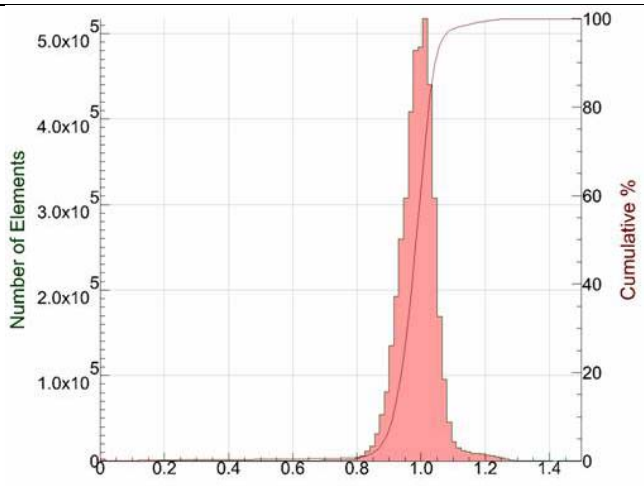

Fig. 9b. Module 41 QE histogram in the H band.

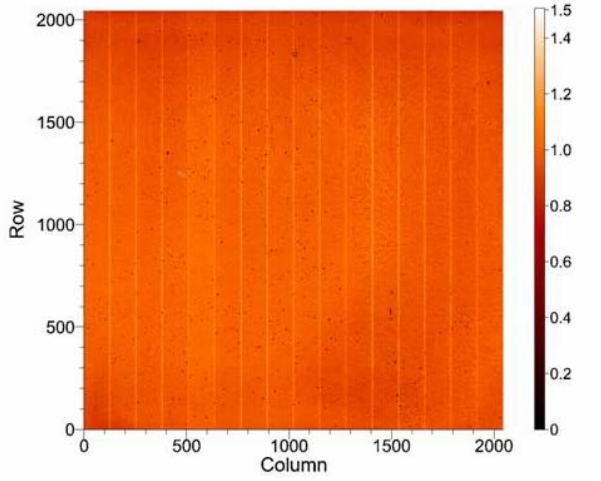

Fig. 10a. Module 41 QE in the K band. The mean QE is 0.980 and the standard deviation is 0.082 (5.6% sigma/ mean). QE operability is 99.73%.

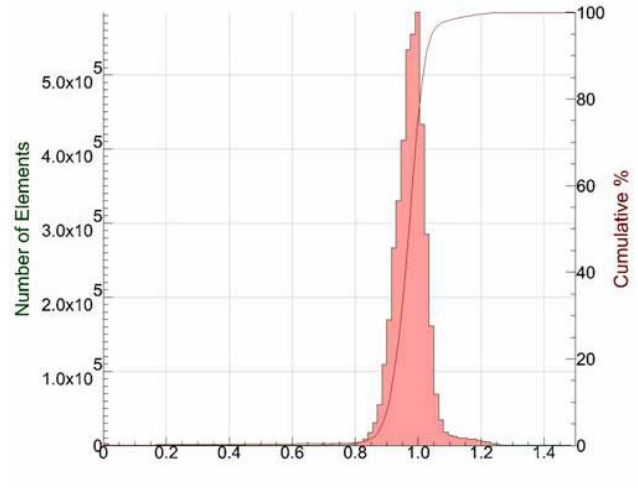

Fig. 10b. Module 41 QE histogram in the K band.

A dark current map and histogram are shown in Figures 11a and 11b, respectively. Dark current was measured at 78 K by sampling up-the-ramp and reading out a total of 10 frames at 120 sec per frame. Dark current was computed from the difference in Dark Signal between frame 10 and frame 4, corresponding to an integration time of 720 sec (12 minute).

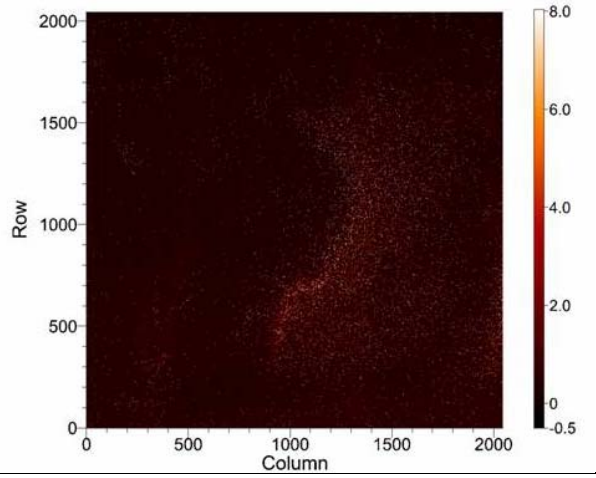

Fig. 11a. Module 41 dark current at 78 K. The mean dark current is 0.38 e-/sec and the standard deviation is 0.55 e-/sec (144 % sigma/mean). Operability is 99.14%.

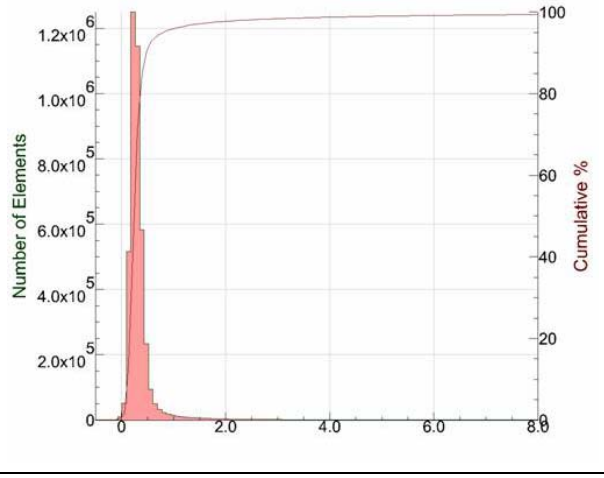

Fig. 11b. Module 41 dark current histogram.

Read Noise is shown in Figure 12. Read Noise was measured using a "pixel-to-pixel" method in which two independent CDS images with a 1.0-second integration time were subtracted from each other on a per-pixel basis. The difference image, when divided by root(2), is used to generate a histogram. The mean of the resulting histogram corresponds to any drift which occurred between the two acquisitions. The standard deviation of the histogram corresponds to the Read Noise. This method is relatively easy and less memory intensive than the "standard" method in which the noise is computed on a per-pixel basis from the temporal standard deviation of each pixel over a series of frames. However, only an array-average noise is derived from this method. The UK ATC has compared the pixel-to-pixel Read Noise and the "temporal" Read Noise and has found good agreement between the two methods.[6]

Figure 13 shows the results of a measurement of conversion gain (transimpedance) using the photon transfer method. The data is based on a 101 × 101 pixel region of the array. From the slope of the linear regression fit, the conversion gain is 3.17 μV/e-. This value was used to input-refer all other output-referred measured parameters. Conversion gain is a function of well depth because, as the SFD input node integrates toward saturation, the detector bias decreases and the detector junction capacitance increases. The increase in capacitance on the input node as full well is approached, results in a slight decrease in the conversion gain. The conversion gain in Figure 13 is representative of the gain obtained at relatively low signal levels. The maximum signal represented in Figure 13 is 137 mV out of a full well of about 500 mV. For module 41, the conversion gain was measured to be 3.99 μV/e-.

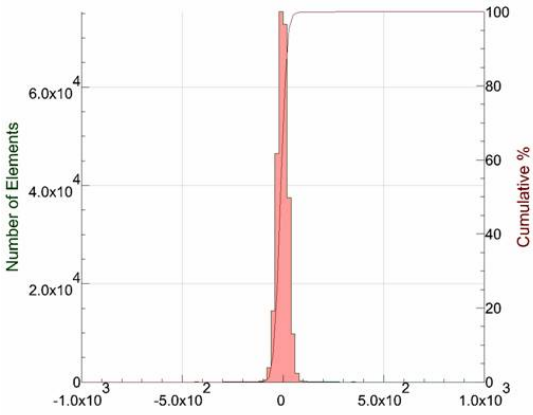

Fig. 12. Module 41 read noise as measured by the "pixel-to-pixel" method. Read Noise is the standard deviation of the histogram and is 25.1 e- rms.

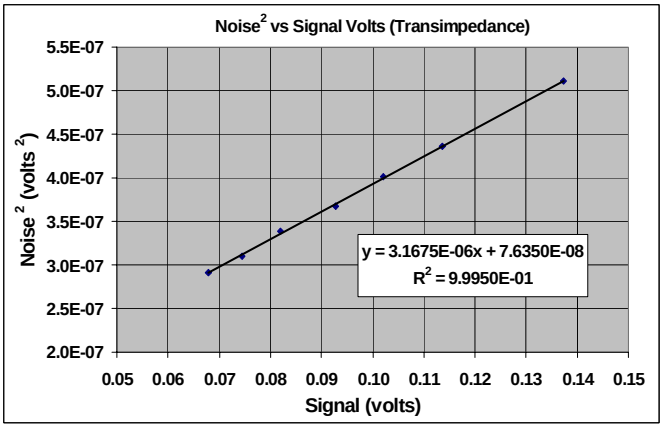

Fig. 13. Module 24 conversion gain as measured by the "photon transfer" method. The measured conversion gain is 3.17 µV/e-.

Detector relative spectral response is illustrated in Figure 14. Spectral response was measured on a non-AR coated Test Structure Assembly (TSA) consisting of a detector test structure hybridized to a sapphire fanout. The detector test structure was physically adjacent to the actual 2K × 2K detector used to fabricate Module 24. The detector 50% cutoff wavelength is 2.54 µm. The response is quite flat between ~0.85 µm, the cut-on wavelength of the detector CdZnTe substrate, and the ~2.5 µm cutoff of the detector.

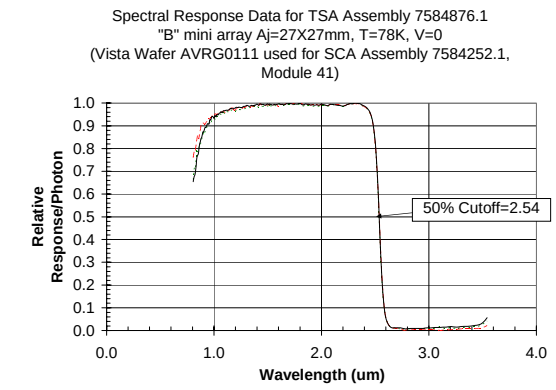

Fig. 14. Module 41 HgCdTe detector relative spectral response measured on a non-AR coated TSA from the same detector wafer.

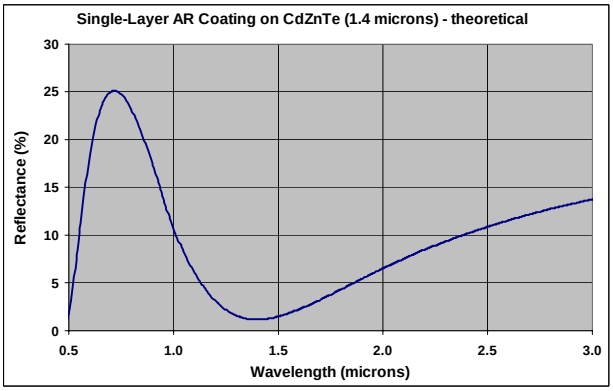

Fig. 15. Single-layer AR coating reflectance spectral (theoretical). The minimum in reflectance was designed to be at a wavelength of 1.4 µm.

An interferogram of Module 41 is shown in Figure 16. Detector flatness is 3.7 µm (peak-to-valley), as measured over 20 points across the array. Module flatness is one of the key requirements of the VISTA program: the detector on each module must be flat to within 12 µm. A map of "open" pixels on module 41 is shown in Figure 17. This data was acquired by performing a Source Follower Gain (SFG) measurement at room temperature in which the detector common bias, VdetCom, was changed by a small amount ΔVdetCom. For detector/ROIC unit cells in which the indium bump are interconnected, the output of the chip will move by an amount ΔVout = Asf*ΔVdetCom where Asf is the total SFG. Conversely, unit cells with no indium bump interconnection will show essentially "zero" SFG. For module 41, the indium bump interconnect was 100%.

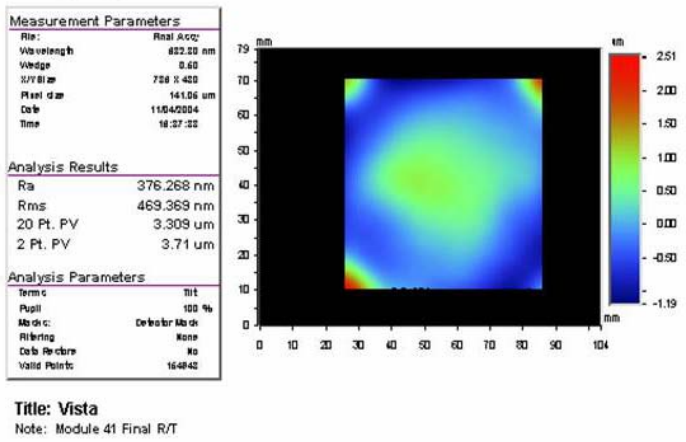

Fig. 16. Module 41 interferogram. The detector flatness is 3.7 µm (peak-to-valley).

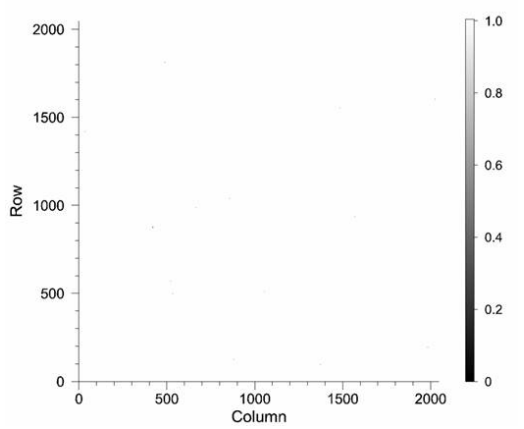

Fig. 17. Pixel "opens" map of module 41. Interconnect operability is essentially 100%. "Black" pixels are "open" and "white" pixels are interconnected.

8. SWIR PV HgCdTe/Si DETECTORS

High performance non-latticed matched HgCdTe grown by MBE on silicon substrates has been demonstrated previously for MWIR HgCdTe/Si detectors tested under tactical conditions[7,8,9]. MWIR detector arrays with operabilities greater than 99 % have been routinely achieved. Expansion of the application for MBE grown materials to SWIR represents a natural synergy, between the larger arrays desired by the Astronomy community and larger available wafer sizes for silicon.

The detector structure is a p-on-n heterojunction diode designed to be compatible with the RVS production line processes. A cross-section of the architecture is shown in Figure 18a along with a processed 4" wafer in Figure 18b. RVS has two MBE growth systems available: a 5" Riber EPINEAT System and a 10" VG-100 system. Wafer grown on substrates up to 6" have been demonstrated. The SWIR material discussed in this paper was grown on 4" silicon substrates in the Riber MBE system and had a 50 % cutoff at 78 K of ~ 2.4 um as measured on a test structure assembly.

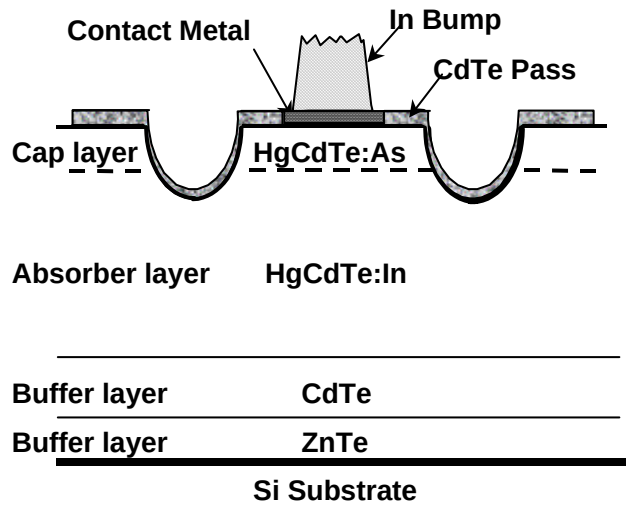

Fig.18a. Representative view of the detector cross section for MBE grown HgCdTe/Si .

Fig. 18b. Picture of a processed 4" HgCdTe grown by MBE on silicon wafer.

9. SCA/MODULE DATA FOR HgCdTe ON Si MODULE 14B

Module 14B uses a MBE grown HgCdTe on Si detector rather than the HgCdTe on CdZnTe substrate which is reported on in earlier sections of the paper. The focal plane testing of such a large array allows multiple analyses to be performed on the detector, including both mean performance and material uniformity. All of the module testing was performed in an identical manner as the VISTA production modules.

Figure 19 shows a histogram of the non AR-coated K-band quantum efficiency (QE). The mean K-band QE (non-AR coated) was 57 % with a sigma/mean of 6%. With an AR coat, the QE is projected to be ~ 73 % with a operability of 99.4 % for the entire 2048 x 2048 array to the VISTA specification. The dark current is shown in Figures 20a and 20b, with 96.2 % of the pixels meeting the VISTA specification and a mean dark current of 0.47 e-/s.

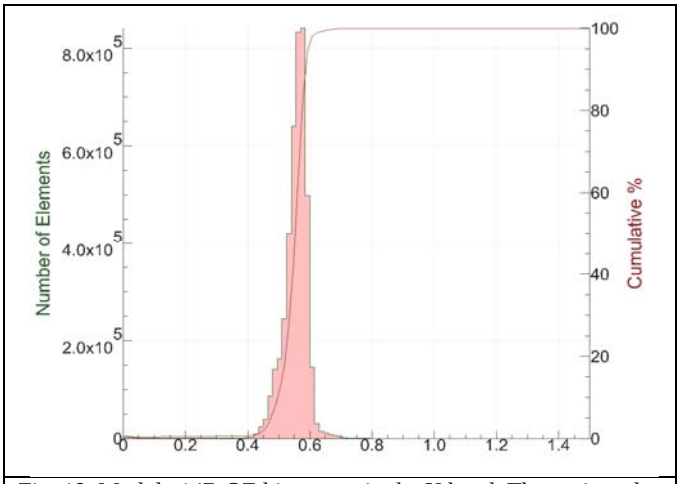

Fig. 19. Module 14B QE histogram in the K band. The projected operability of the array with an ARC is 99.4 %.

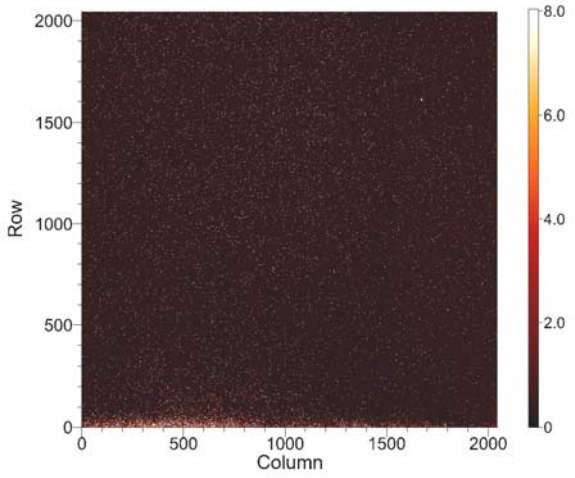

Fig. 20a. Module 14B dark current. The mean dark current is 0.47 e-/s. The dark current operability is 96.2 %.

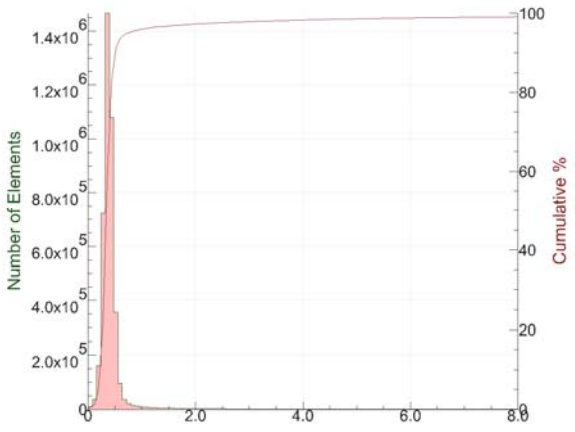

Fig. 20b. Module14B dark current histogram.

10. SUMMARY

Raytheon Vision Systems has expanded the Astronomy product line with the introduction of the VIRGO 2Kx2K, 20 mm ROIC for low-background astronomy applications. Such large arrays utilize and demonstrate the uniformity of the RVS HgCdTe production line necessary to achieve high yields for smaller arrays. Although designed specifically for VISTA, which utilizes SWIR HgCdTe detectors with a cutoff wavelength of ~2.5 microns operating at ~80 K, the VIRGO ROIC is compatible with a variety of detectors, including HgCdTe with other cutoff wavelengths, InSb and Si PIN detectors.[10] The ROIC can be fabricated in integer multiples of a basic 512 × 1024 building block and is designed to be 3-side buttable to facilitate fabrication of large mosaics of 4K × 2nK format. The HgCdTe/CdZnTe detectors have high QE and flat response over the wave-band of interest. With a suitable AR coating, QE in excess of 90% can be achieved over a wide wavelength range. The lower wavelength limit of the pass-band, about 0.85 microns, is determined by the cut-on wavelength of the wide band-gap CdZnTe detector substrate. For applications which require visible as well as NIR response, a technique is currently under development which completely removes the substrate after hybridization, allowing visible response down to ~0.4 microns.

A robust and reliable 3-side buttable module package has been developed for the 2K × 2K SCA which provides a simple "plug-and-play" interface. Thermal cycle reliability is excellent, with more than 200 thermal cycles between ambient and 80 K demonstrated to date with no loss in pixel operability.

The VISTA program has been completed, with delivery of 2 engineering modules and 16 science grade modules. All VISTA performance requirements at 80 K were met with significant margin: QE > 70% in all spectral bands (with single-layer AR coating), read noise < 20 electrons rms with off-chip CDS, and dark current < 4 electrons/sec for a cutoff wavelength of 2.5 microns at 80 K.

With the need for larger detectors exceeding the physical size of the CdZnTe substrates, RVS has demonstrated near spec performance of SWIR HgCdTe detectors grown by MBE on silicon substrates. Projected AR coated QE's > 70 % with operabilites of 99.4 % and dark currents less then 1 e-/s have been achieved.

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10. REFERENCES

1. D. J. Gulbransen, P. J. Love, M. P. Murray, N. A. Lum, C. L. Fletcher, E. Corrales, R. E. Mills, A. W. Hoffman, K. J. Ando, "Megapixel and Larger Readouts and FPAs for Visible and Infrared Astronomy", in *Proc. SPIE, Instrument Design and Performance for Optical/Infrared Ground-based Telescopes*, M. Iye and A. F. M. Moorwood, editors, **4841**, pp. 395-404, 25-28 Aug., 2002.
2. J.P. Emerson, "VISTA - Project Status of the Visible and Infrared Survey Telescope for Astronomy", in *The New Era of Wide Field Astronomy, ASP Conference Series. ed. R. Clowes, et al. San Francisco: Astronomical Society of the Pacific.*, **232**, pp 339-342, 2001.

3. J.P. Emerson and W. Sutherland, “Visible and Infrared Survey Telescope for Astronomy: Overview”, in *Proc. SPIE, Survey and Other Telescope Technologies and Discoveries*, J. A. Tyson, S. Wolff, editors, **4836**, pp. 35-42, 2002.
4. A. M. McPherson, S. Craig, W. Sutherland, “Project VISTA, a review of its progress and overview of the current programme”, in *Proc. SPIE, Large Ground-based Telescopes*, J. M. Oschmann, L. M. Stepp, editors, **4837**, pp. 82-93, 2003.
5. P. J. Love, A. W. Hoffman, D. J. Gulbransen, M. P. Murray, K. J. Ando, N. J. Therrien, J. P. Rosbeck, R. S. Holcombe, “Large-Format 0.85 - 2.5 Micron HgCdTe Detector Arrays for Low-Background Applications”, in *Proc. SPIE, Focal Plane Arrays for Space Telescopes*, T. J. Grycewicz and C. R. McCreight, editors, **5167**, pp 134-143, 4-6 Aug., 2003.
6. N. Bezawada, D. Ives, G. Woodhouse, “Characterization of VISTA IR Detectors”, in *Proc. SPIE, Optical and Infrared Detectors for Astronomy*, J. W. Beletic and J. D. Garnett, editors, **549**9, 21-22 June, 2004.
7. J.M. Peterson, et. al., “MBE HgCdTe Growth on 4-inch Substrates for Large Format MWIR Focal Plane Arrays,” MSS March 2001 Proceedings
8. A. Childs, J. Varesi, K. Maranowski, J. Peterson, L. Giegerich, R. Bornfreund, S. Johnson, and W. Radford, “Advancements in Large Area MBE grown HgCdTe/Si Detectors and FPAs,” MSS March 2001 Proceedings
9. R. Bornfreund, A. Childs, J. Varesi, J. Graham, J. Peterson, A. Buell, S. Johnson, D.F. King, and W. Radford, “Development Status for MBE grown HgCdTe on Si Detectors and FPAs”, MSS February 2003 Proceedings
10. A. W. Hoffman, P. J. Love, and J. P. Rosbeck, “Mega-Pixel Detector Arrays: Visible to 28 μm," in *Proc. SPIE, Focal Plane Arrays for Space Telescopes*, T. J. Grycewicz and C. R. McCreight, editors, **5167**, pp194-203, 4-6 Aug., 2003.